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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION - PHASE II

BIPOLAR NAND GATE STUDY

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST

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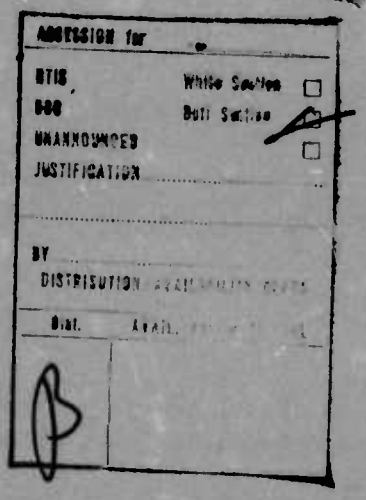
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SUBMITTED TO:
CONTRACTING OFFICER
U.S. NAVAL WEAPONS LABORATORY
DAHLGREN, VA. 22448
CONTRACT NO. N00178-73-C-0362

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST
Saint Louis, Missouri 63166 (314) 232-0232

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PREFACE

This document is one of eight task-oriented reports prepared under Contract No. N00178-73-C-0362 for the U. S. Naval Weapons Laboratory, Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company personnel involved were:

J. M. Roe, Study Manager

J. R. Chott

C. E. Clous

V. R. Ditton

T. A. Niemeier

G. W. Renken

R. D. Von Rohr

J. A. Waite

This report was reviewed by J. R. Cummings.

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1. INTRODUCTION AND SUMMARY

The Integrated Circuit (IC) Electromagnetic Susceptibility Investigation is a part of a much larger effort at the U. S. Naval Weapons Laboratory (NWL) entitled the Electromagnetic Vulnerability Assessment Program (EMVAP). EMVAP covers all aspects of the electromagnetic vulnerability problem from test and evaluation to research and development into underlying phenomena. The research and development activities have been divided into three mutually interdependent areas: environment definition, EM coupling, and component susceptibility. The component susceptibility investigations are performed by direct injection of RF energy into the terminals of the device, i.e., a hard-line connection from the RF source to the component. Discrete component susceptibility is investigated as an in-house effort at NWL, and integrated circuit susceptibility is studied by McDonnell Douglas Astronautics Company - East (MDAC-E) as a contracted activity. The work reported herein is part of a Phase II contracted effort which builds upon a previous Phase I contract also performed by MDAC-E.

The main thrust of Phase II of the Integrated Circuit Electromagnetic Susceptibility Investigation has been to develop a model of the effects that occur in bipolar integrated circuits. The broad category of bipolar devices was subdivided into digital and linear with a bipolar operational amplifier representing the linear subcategory reported on elsewhere [1]. A 7400-2-input NAND gate was selected as a representative digital device for intensive study to develop the investigation techniques and to explore the basic physics of the RF interaction with the semiconductor device itself. This report documents the digital study and the results show wider ranging implications than for the bipolar NAND gates alone.

In particular, the basic mechanism of RF interaction is shown to be rectification on both the functional and parasitic pn junctions of the device. Those junctions which are directly across the RF voltage source contribute the

largest effects while junctions imbedded inside the chip are affected by an attenuated RF signal which couples across, through, or around various obstacles such as back-to-back junctions and parasitic capacitances. The rectifying junctions can be modelled as Norton or Thevenin equivalent circuits with empirically determined parameters, and it is shown that relatively simple circuit analysis yields not only an understanding of the manifestations of RF effects on the 7400 circuit operation, but also indicates the possibility of easily-implemented design techniques or device screening procedures for reducing circuit susceptibility in other similar devices.

While a clear picture of the first order effects has been verified in the 7400 NAND gate, it is not clear if higher order effects (as observed in the 7400) will dominate in other devices with such variables as junction, chip layout, and manufacturer. It is therefore recommended that investigations into these variables be carried out.

2. MEASURED RF EFFECTS IN THE 7400 NAND GATE

Both non-destructive interference tests and catastrophic failure tests were performed on the 7400 NAND gate. For our purposes, interference is defined as an RF-induced effect which disappears when the RF stimulus is removed. Catastrophic failure is defined as a permanent physical damage (burnout) which prevents the device from functioning at all. The catastrophic failure data was collected primarily to identify failure mechanisms and to establish preliminary failure threshold levels which, in general, are several orders of magnitude higher than the interference level.

2.1 Interference Effects - Changes in various device operational parameters were observed over a wide range of experimental conditions. The changes ranged from barely perceptible pertubations to complete changes in the device logic state. This section will describe the test plan and the observed data.

2.1.1 Interference Test Plan - The 7400 NAND gate is a TTL medium-speed, high noise immunity, saturating logic gate. The chip itself contains four 2-input NAND gates. A schematic diagram of one of these gates is shown in figure 1. A photograph showing the layout of the discrete elements used to make up one of these gates is shown in figure 2. This gate is designed to recognize, at the input, 0.8 volts or less as a logic low, and 2.0 volts or more as a logic high. Figure 3 illustrates these two levels and shows the noise margins associated with these states. More detailed information about the gate can be obtained by referencing a TTL integrated circuit handbook.

The general philosophy of the test plan was to gather a data base from which basic physical mechanisms could be inferred. Previous results [2] had indicated the need for monitoring many parameters simultaneously to insure that a complete picture of what happens to the device under test would be available for detailed analysis.

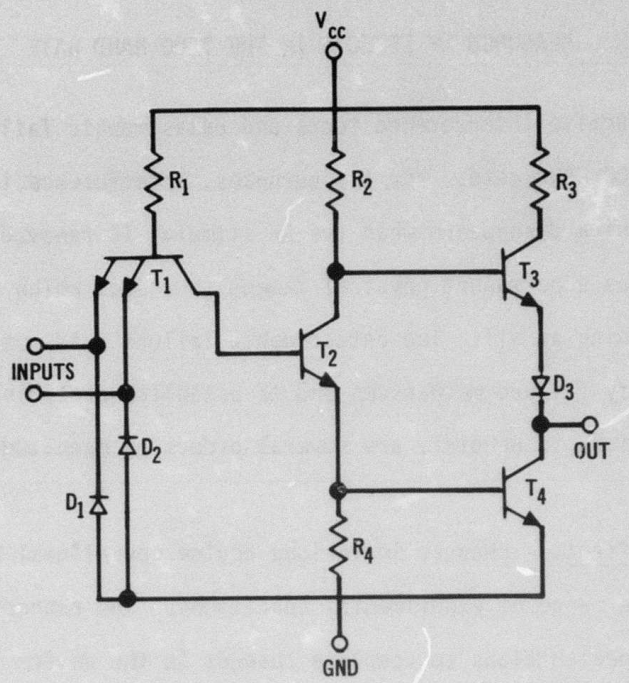


FIGURE 1 SCHEMATIC DIAGRAM OF NAND GATE

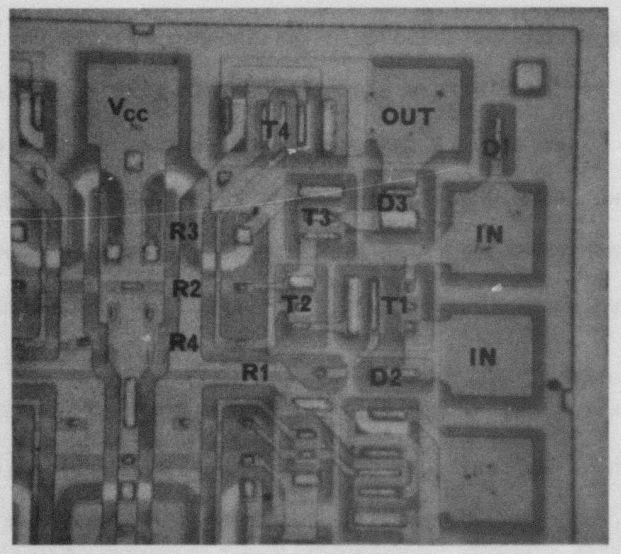


FIGURE 2 PHOTOGRAPH OF THE NAND GATE SHOWING CHIP LAYOUT OF DISCRETE ELEMENTS

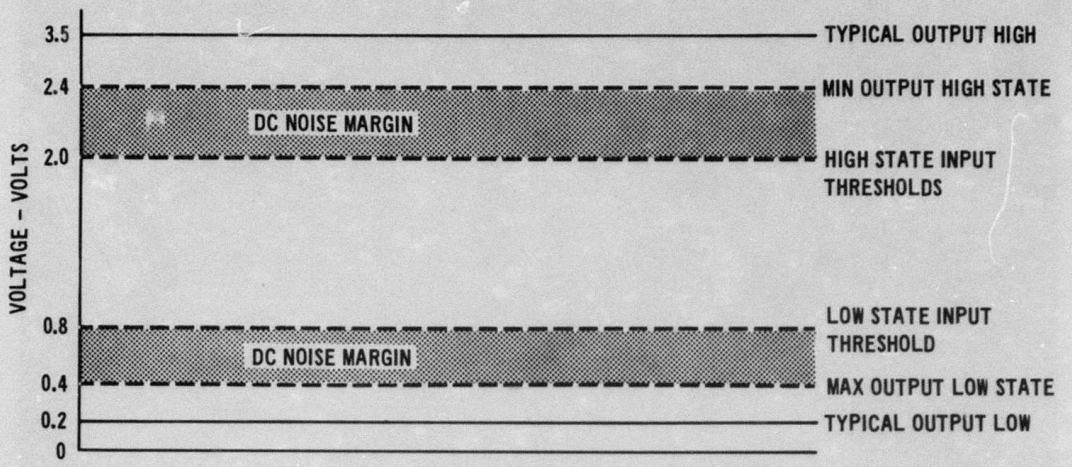


FIGURE 3 DIAGRAM INDICATING TYPICAL LOGIC LEVELS RECOGNIZED BY A TTL 7400 NAND GATE

Accordingly, a sophisticated measurement system was developed to permit a large number of measurements to be made under computer control [3]. The heart of this measurement system is a specially-designed test fixture permitting accurate control and monitoring of the RF stimuli used to stress the device under test, while simultaneously permitting bias voltages and currents to be supplied to the device. Figure 4 is a photograph of the test fixture, and figure 5 shows a block diagram of the overall test setups as used in the 7400 interference tests. A complete description of the fixture and test setup is given in reference 3.

The basic test plan was to inject an RF signal into each of the four ports (input, output, V_{CC}, and ground) of one of the gates on the chip for each combination of frequency and bias state. The two input terminals were tied together for all of the tests so that two bias states were possible: output high and output low. There were five test frequencies: 0.22, 0.91, 3.0, 5.6, and 9.1 GHz. There were, therefore, 40 different test conditions (4 ports x 5 frequencies x 2 bias states). For each test condition, 10 samples were used to establish the range of device-to-device

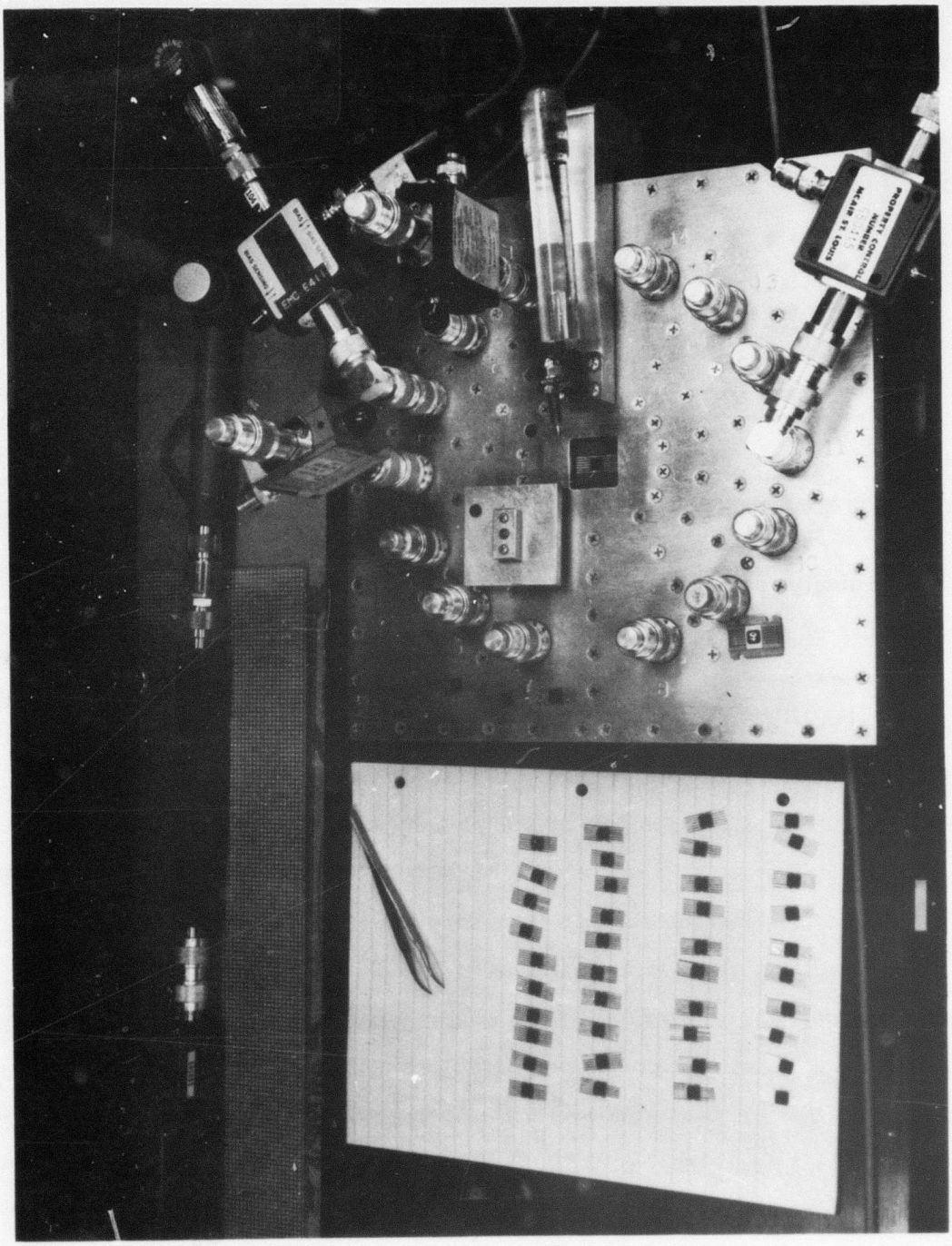


FIGURE 4 PHOTOGRAPH OF TEST FIXTURE

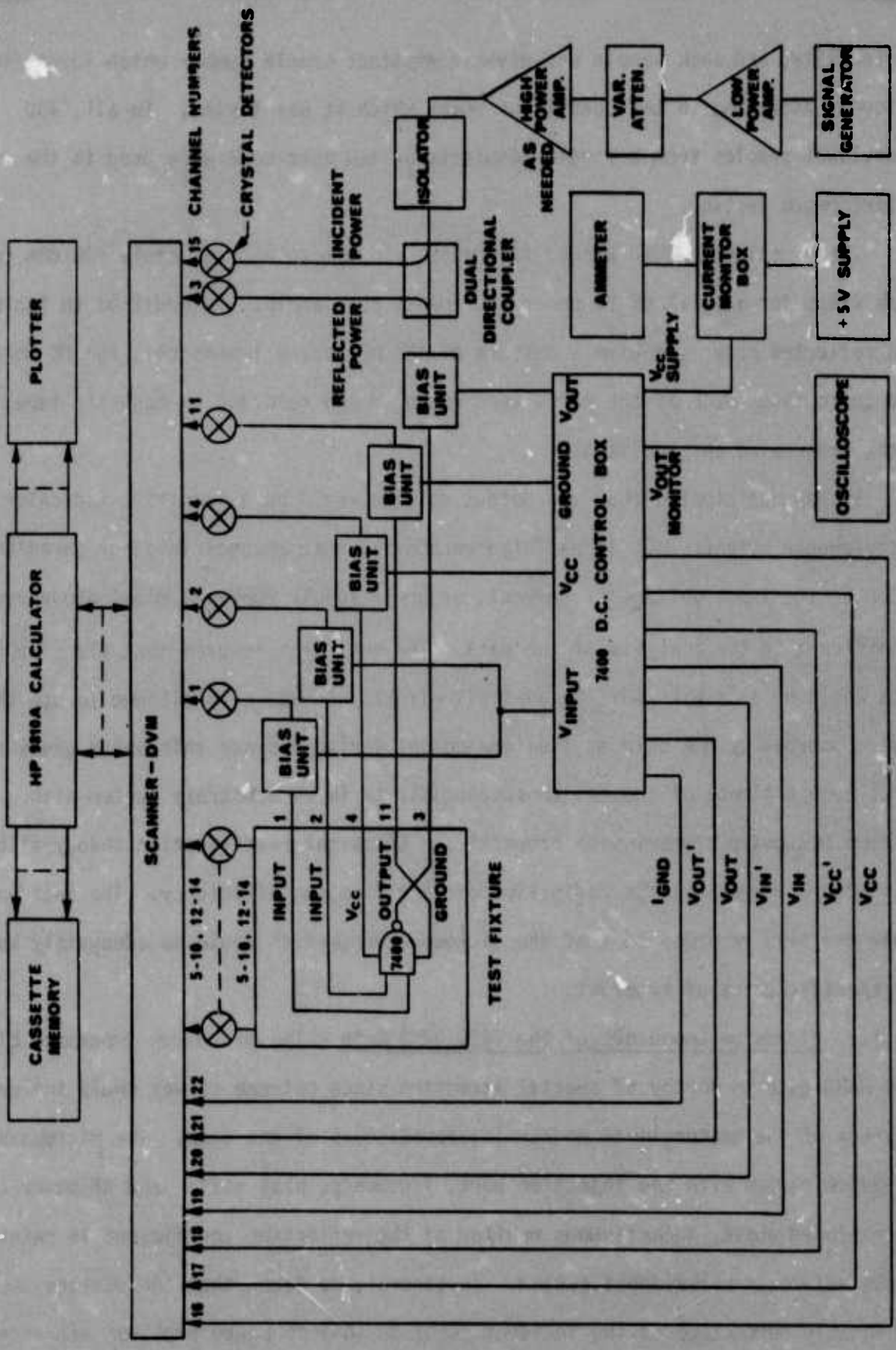


FIGURE 5 BLOCK DIAGRAM OF 7400 TEST SETUP

variability, and each sample was given a distinct sample number which identified it uniquely according to the conditions under which it was tested. In all, 400 individual samples from a single manufacturer and date-code were used in the interference testing.

The RF stimulus used ranged from about -10 dBm to approximately +30 dBm in 2 dB steps for a total of 20 power increments per sample. In addition to incident and reflected power (to give a measure of the microwave impedance), the DC voltages and currents at each of the ports were measured and recorded on magnetic tape for later processing and analysis.

It was anticipated that the output voltage would be a sensitive indicator of interference effects, but it was also recognized that changes in other parameters (such as the input voltage or current, or power supply current) might prove very significant in the analysis of the data. The test plan insured that all of this data would be available for the analysis effort. It was also planned to use the power absorbed by the chip as the independent variable since this value gives a worst-case estimate of the device susceptibility in an arbitrary system with unknown microwave transmission properties. Classical rectification theory also uses absorbed power in the definition of rectification efficiency. The incident power was also recorded so that the microwave properties could be adequately known for specific cases of interest.

2.1.1.1 Microwave Impedance of the 7400 NAND Gate - The microwave impedance of the 7400 NAND gate is worthy of special attention since extreme values could influence accuracy of the measurements and/or interpretations of the data. The microwave impedance varies with the injection port, frequency, bias state, and RF power level. As mentioned above, a continuous monitor of the reflection coefficient is maintained by the automatic measurement system. In general, we found that the devices absorb a respectable percentage of the incident power so that no undue problems are encountered

with respect to measurement accuracy or equipment capability (the power reflected, in effect, reduces the power available from the test equipment to stress the device). Figure 6 shows the derived reflection coefficient for the device input port.

The reflection coefficient can be translated to a range of impedance magnitudes, and this is sufficient for most purposes. It is of interest, however, to look at the complex impedance of the device. A series of swept frequency measurements of the input and output impedances were made for three different power levels at the two bias states and the data is summarized in Table 1. It can be seen that the impedances are not extreme which bears out the conclusions derived from the reflection coefficient data.

2.1.2 Interference Data - The interference data taken can be divided into two major groups, those of direct or indirect effects. Direct effects are those RF effects experienced at the port of RF entry, and indirect effects are those RF effects observed at ports other than the port of RF entry. An example of a direct effect would be an observed change in the input voltage as a result of RF entering the input port. On the other hand, an example of an indirect effect would be a change-in-state of the output as a result of RF entering some other port. The data was further divided into four major categories according to bias state and port of RF entry. Figure 7 lists these categories. Each of these categories will be discussed in one of the following sections. In order to limit the scope of the discussions, it should be mentioned that as frequency increased, the RF interference effects diminished. An example demonstrating this trend is shown in figure 8. Since the RF effects diminish with increasing frequency, the following discussions utilize the interference data collected at 0.22 GHz (as this would then be the most significant example).

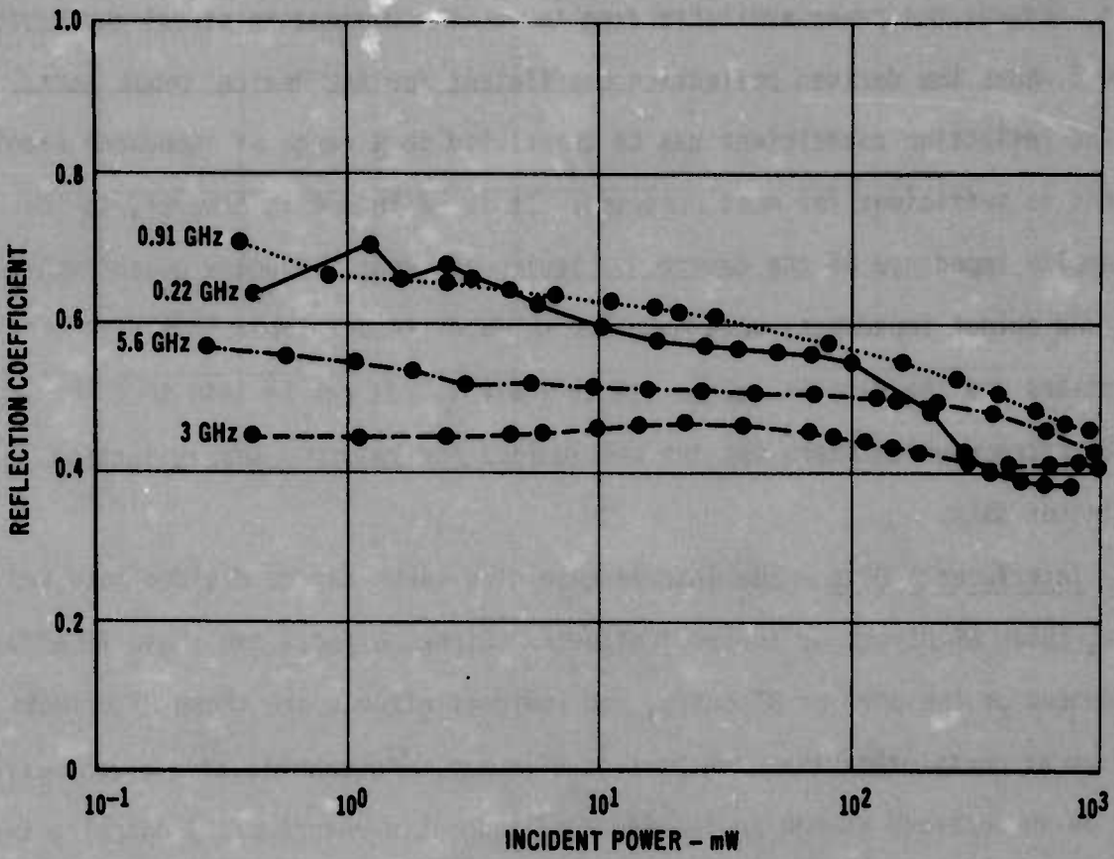


FIGURE 6 PLOT OF DERIVED REFLECTION COEFFICIENT FOR THE DEVICE INPUT PORT

TABLE 1 MICROWAVE IMPEDANCE OF A 7400 NAND GATE AT 10 mW

	PORT / BIAS STATE	INPUT PORT Z (Ω)	OUTPUT PORT Z (Ω)
3.0 GHz	HIGH	$(82.5 \pm 19.7) - j\,(50.3 \pm 7.6)$	$(19.7 \pm 2) - j\,(11.5 \pm 3.1)$
	LOW	$(37.9 \pm 3.5) - j\,(25.8 \pm 3.8)$	$(23.4 \pm 2.9) - j\,(27.7 \pm 3.6)$
9.1 GHz	HIGH	$(46.3 \pm 1.9) + j\,(68 \pm 4.0)$	$(78.5 \pm 2.4) + j\,(112.5 \pm 2.6)$
	LOW	$(39 \pm 1.0) + j\,(67.7 \pm 2.9)$	$(97 \pm 4.2) + j\,(121 \pm 2.1)$

CATEGORY OF DATA DISCUSSED IN SECTION	RF INJECTED ON		BIAS STATE			
	INPUT PORT	OUTPUT PORT	INPUT LOW	INPUT HIGH	OUTPUT LOW	OUTPUT HIGH
2.1.2.1	X		X			X
2.1.2.2	X			X	X	
2.1.2.3		X		X	X	
2.1.2.4		X	X			X

FIGURE 7 CATEGORIES OF DATA DISCUSSED IN THE REPORT

2.1.2.1 RF Entering the Input With Input Low - For this particular set of test conditions, the two most dominant RF effects were: 1) the input current drastically increased with RF power, and 2) the output changed state (from the high to the low state). Graphs of the input current and output voltage versus RF power absorbed are shown in figures 9 and 10, respectively.

2.1.2.2 RF Entering the Input With Input High - The major effect under these conditions was a current flowing into the device (figure 11). No other significant effects were observed.

2.1.2.3 RF Entering the Output With Output Low - The major effect observed under these conditions was a change-in-state of the output voltage. The switch was from a logic low to logic high state. A plot of the output voltage is shown in figure 12.

2.1.2.4 RF Entering the Output With Output High - The major interference effect observed under these test conditions was an increase in the output voltage. However, no change-in-state occurred as the device was biased to operate in the high output state. A plot of the output voltage is shown in figure 13.

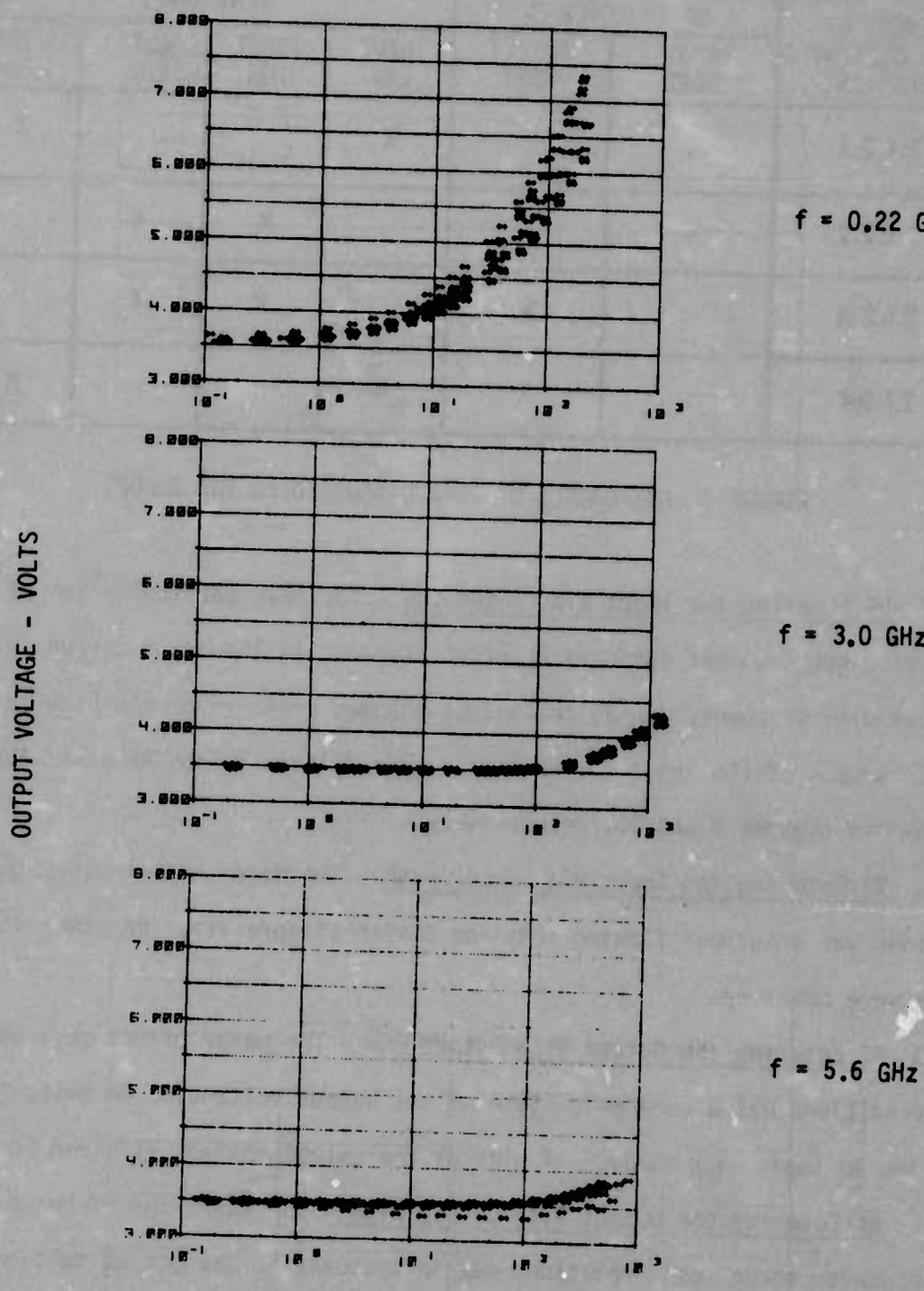


FIGURE 8 ILLUSTRATION OF FREQUENCY EFFECTS
RF INJECTED ON OUTPUT - OUTPUT HIGH

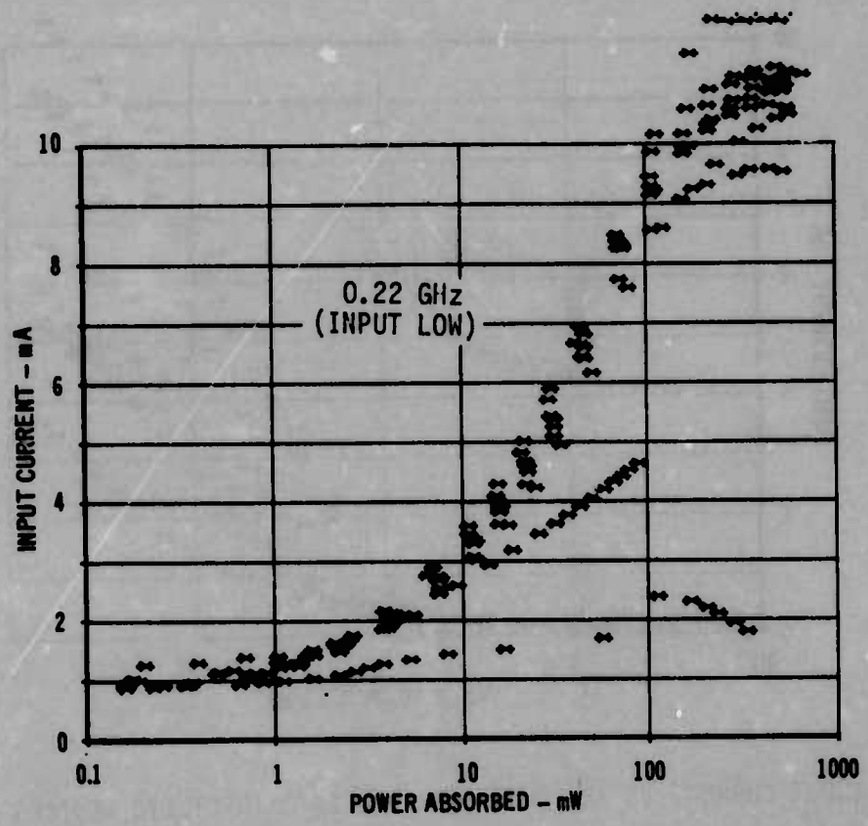


FIGURE 9 INPUT CURRENT VS RF POWER INJECTED INTO INPUT (10 DEVICES SHOWN)

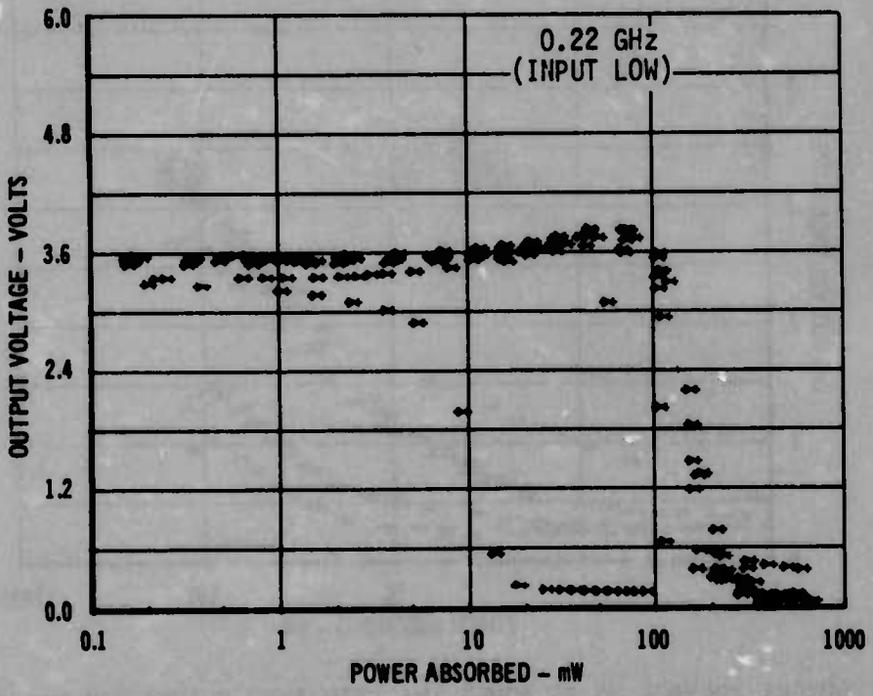


FIGURE 10 OUTPUT VOLTAGE VS RF POWER INJECTED INTO INPUT (10 DEVICES SHOWN)

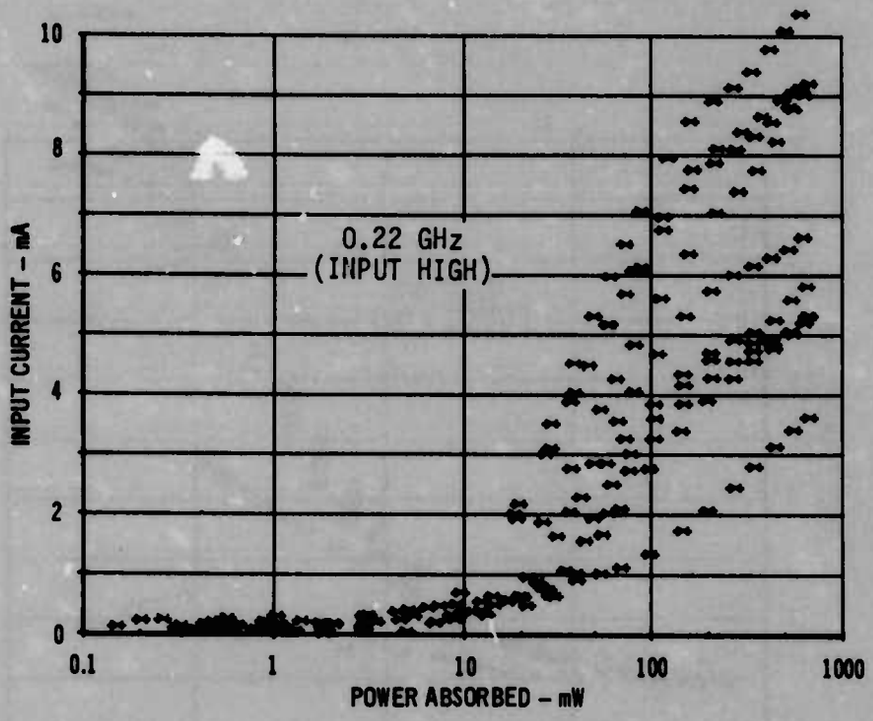


FIGURE 11 INPUT CURRENT VS RF POWER INJECTED INTO INPUT (10 DEVICES SHOWN)

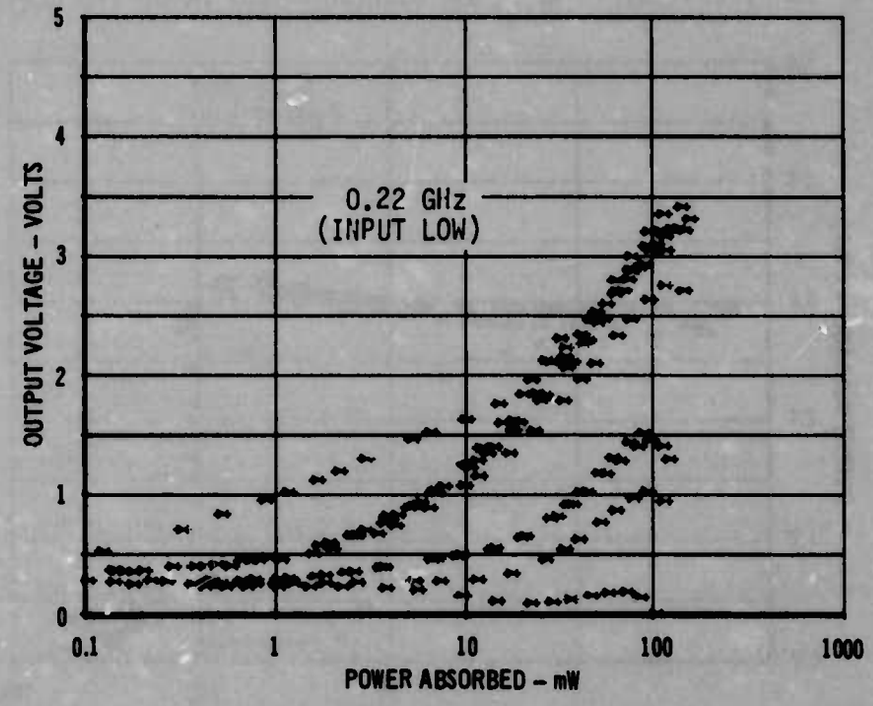


FIGURE 12 OUTPUT VOLTAGE VS RF POWER INJECTED INTO OUTPUT (10 DEVICES SHOWN)

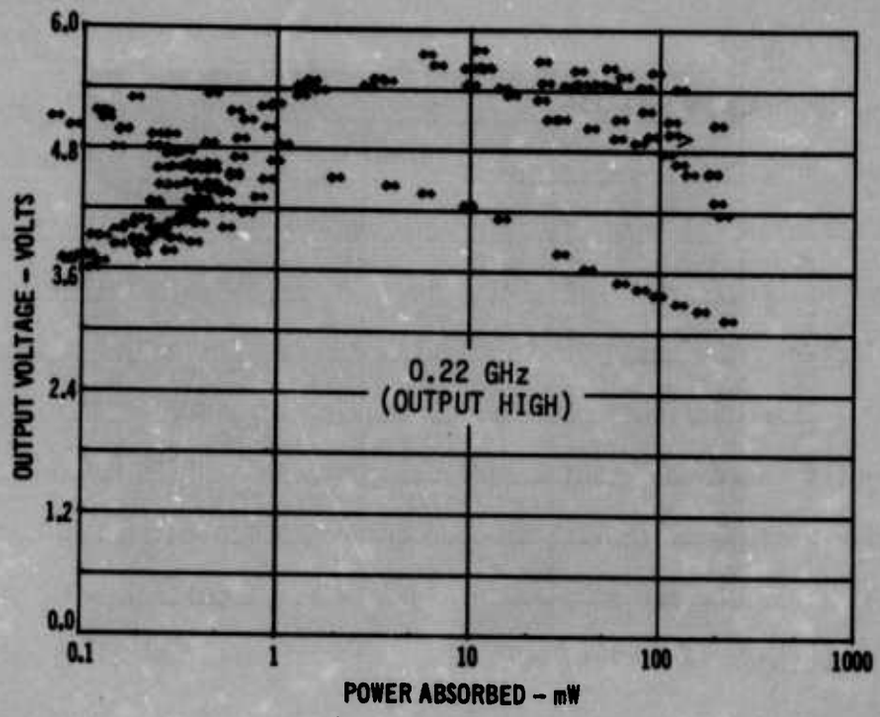
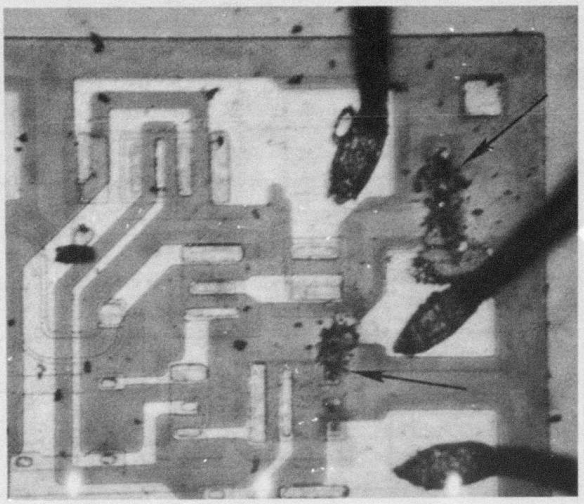


FIGURE 13 OUTPUT VOLTAGE VS RF POWER INJECTED INTO OUTPUT (10 DEVICES SHOWN)

2.2 Degradation and Failure Effects - No degradation effects were observed in the 7400. Catastrophic failure testing performed on the 7400 established the failure threshold for various injection-port/bias-state/frequency combinations. Analysis of the failure data has also been helpful in locating RF paths, and in some instances, added insight in locating probable sites for the interference generators. Some of the failure mechanisms observed include input transistor and diode failures (see figure 14), output transistor failure (see figure 15), ground bond lead failure (see figure 16), and a chain of failures from the V_{cc} connection through to the output (see figure 17).



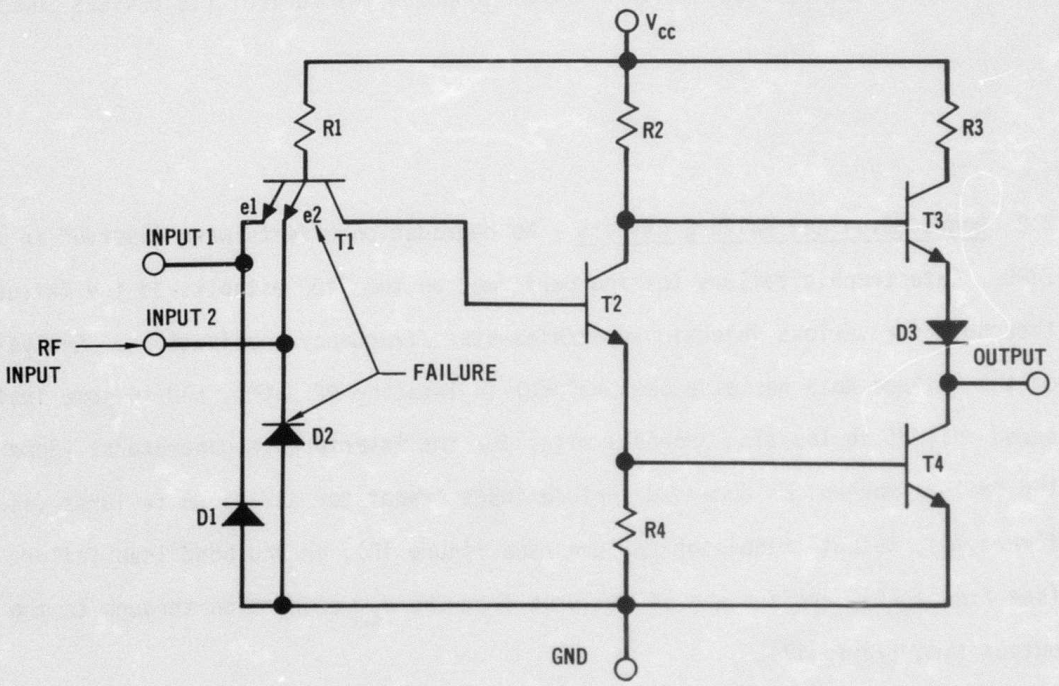
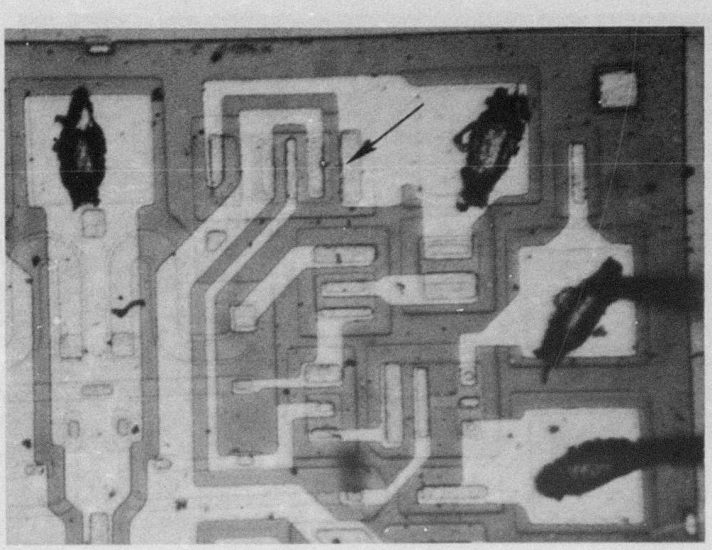


FIGURE 14 INPUT TRANSISTOR AND DIODE FAILURE OF 7400 DEVICE



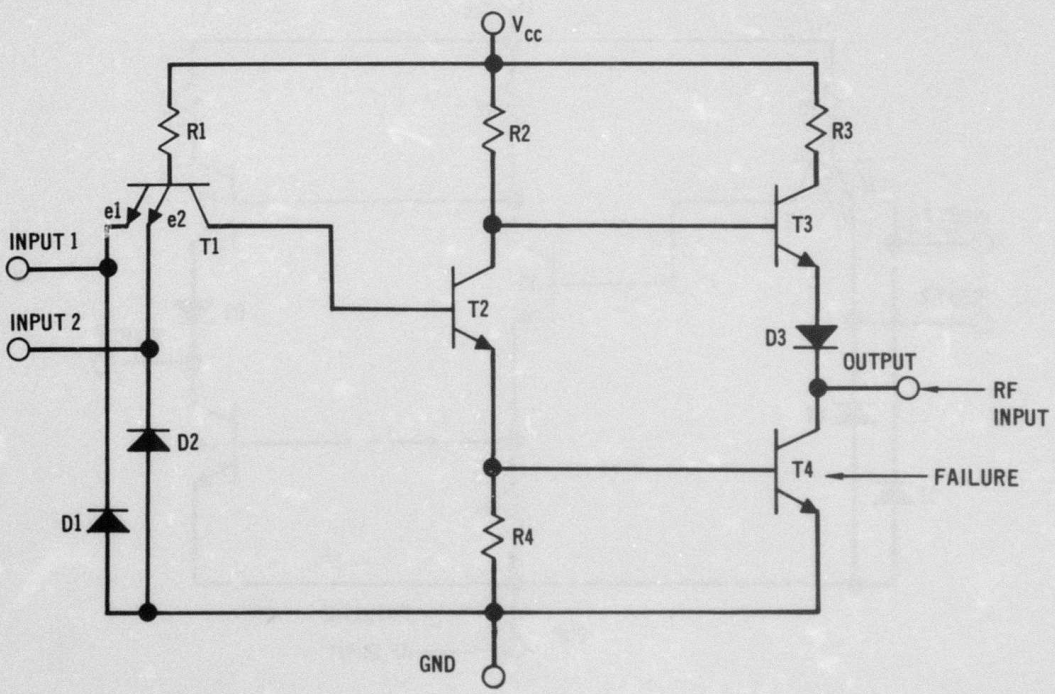
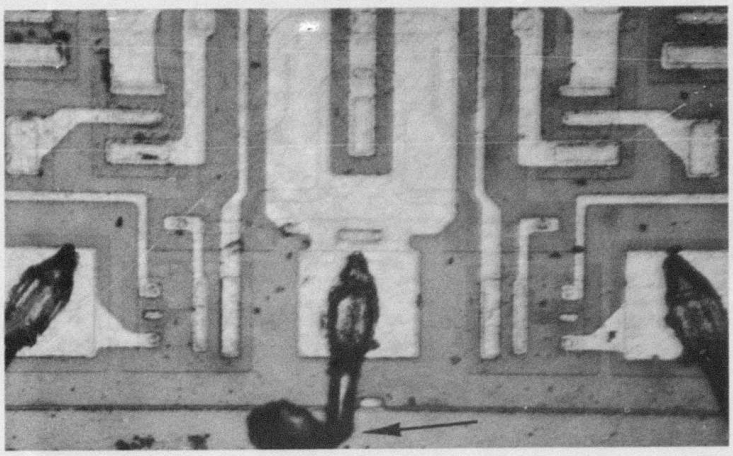


FIGURE 15 OUTPUT TRANSISTOR FAILURE OF 7400 DEVICE



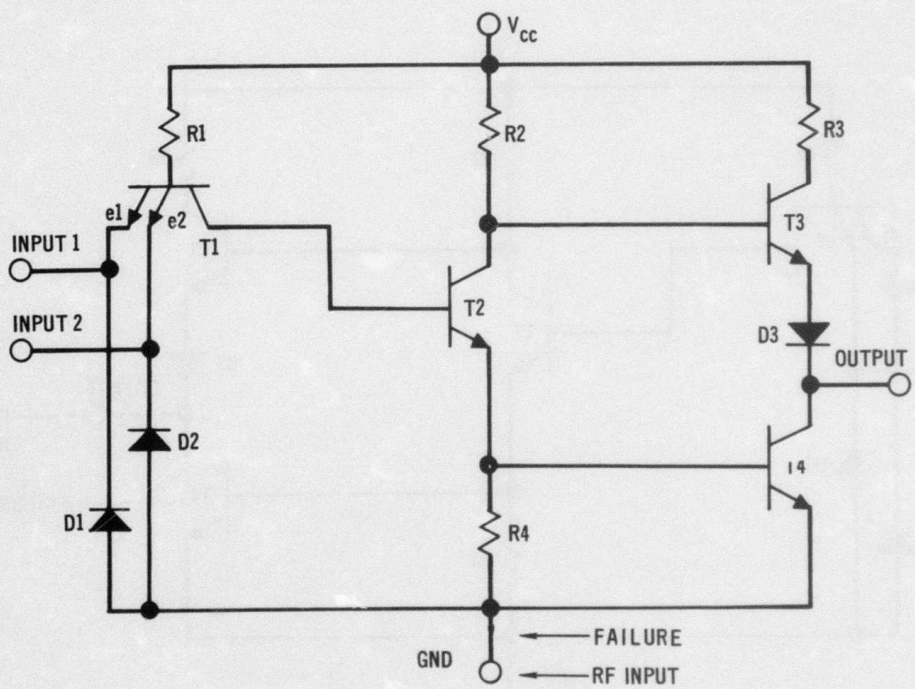
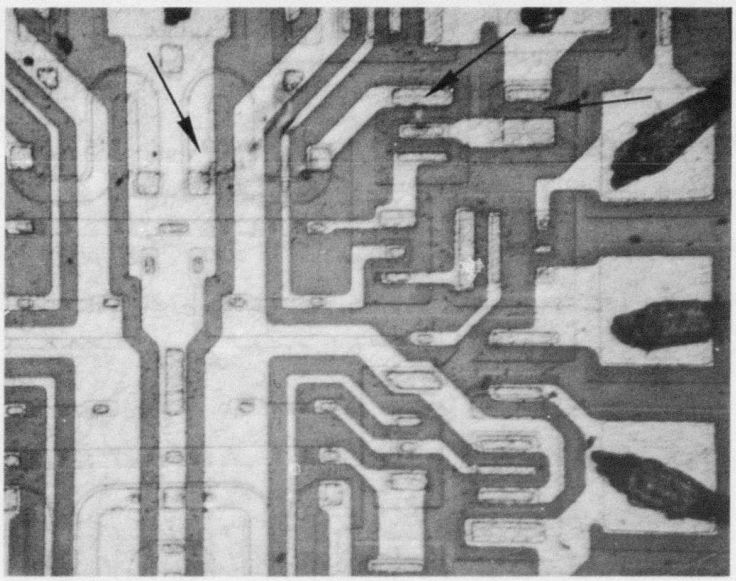


FIGURE 16 GROUND BOND LEAD FAILURE OF 7400 DEVICE



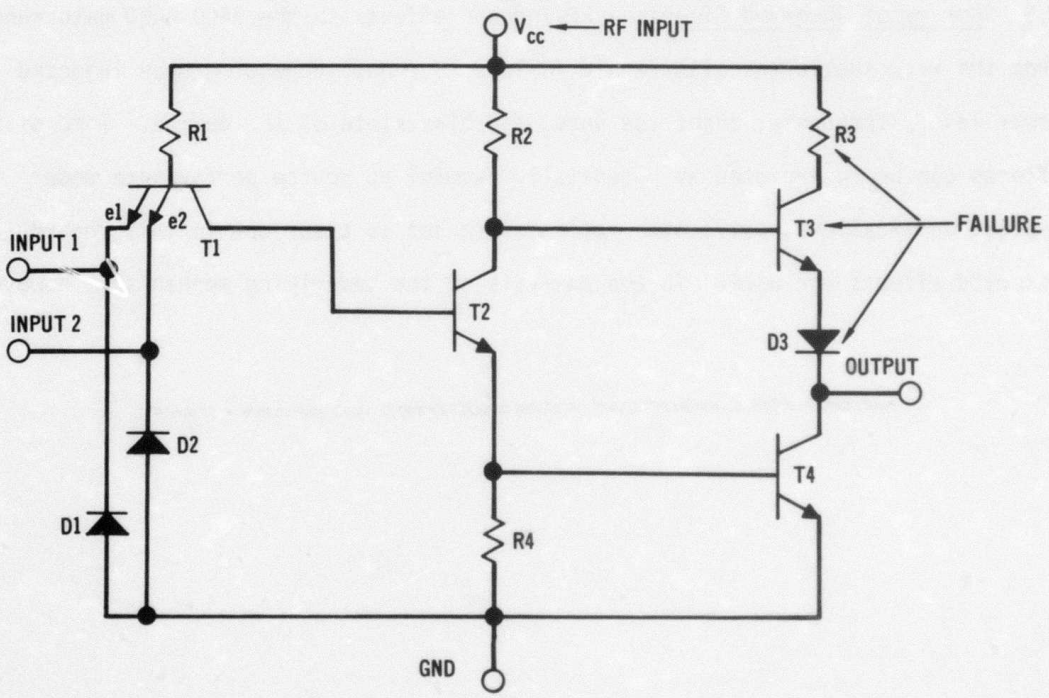


FIGURE 17 CHAIN OF JUNCTION FAILURES OF 7400 DEVICE

The experimental procedure for measuring failure thresholds uses the Bruceton technique in which each device receives a single stress (a 500 μsec pulse in our case) whose strength is determined by the previous result. Thus, the succeeding stimulus is increased one decibel if no failure occurs, and is decreased one decibel for the next device if a failure is observed. This procedure tends to bracket the mean failure level and leads to about 50% failed devices and 50% non-failed devices. It is also possible to estimate the standard deviation from the data.

Figures 18 through 21 show the measured thresholds. The mean failure level (i.e., the power level at which 50% of the samples failed) is plotted with brackets indicating $\pm 1\sigma$. A few instances are plotted in which it was not possible to obtain failure up to the limit indicated. Altogether, 800 individual samples were tested with 178 failures produced.

2.3 Summary of Observed Effects - RF-induced effects in the 7400 NAND gate range from the very subtle to catastrophic failure (burnout) depending upon injected power level, frequency, injection port, and bias state of the device. Some of the effects can be interpreted as potentially harmful to device performance under typical applications, while other effects are not so clear cut in this regard. All observed effects are useful in the analysis of the underlying mechanisms, however.

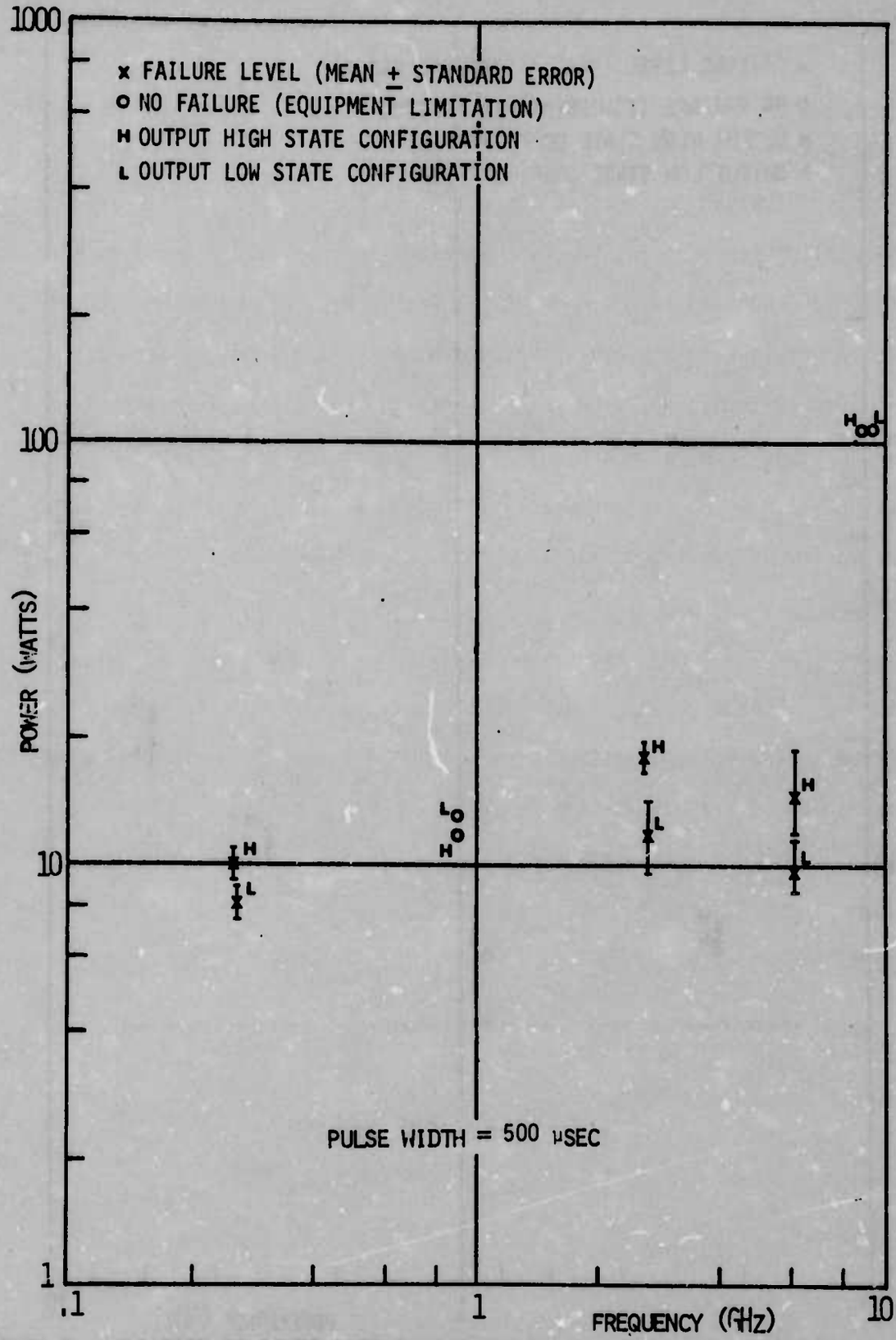


FIGURE 18 ABSORBED RF POWER INTO CHIP REQUIRED TO CAUSE CATASTROPHIC FAILURE AT THE INPUT PORT

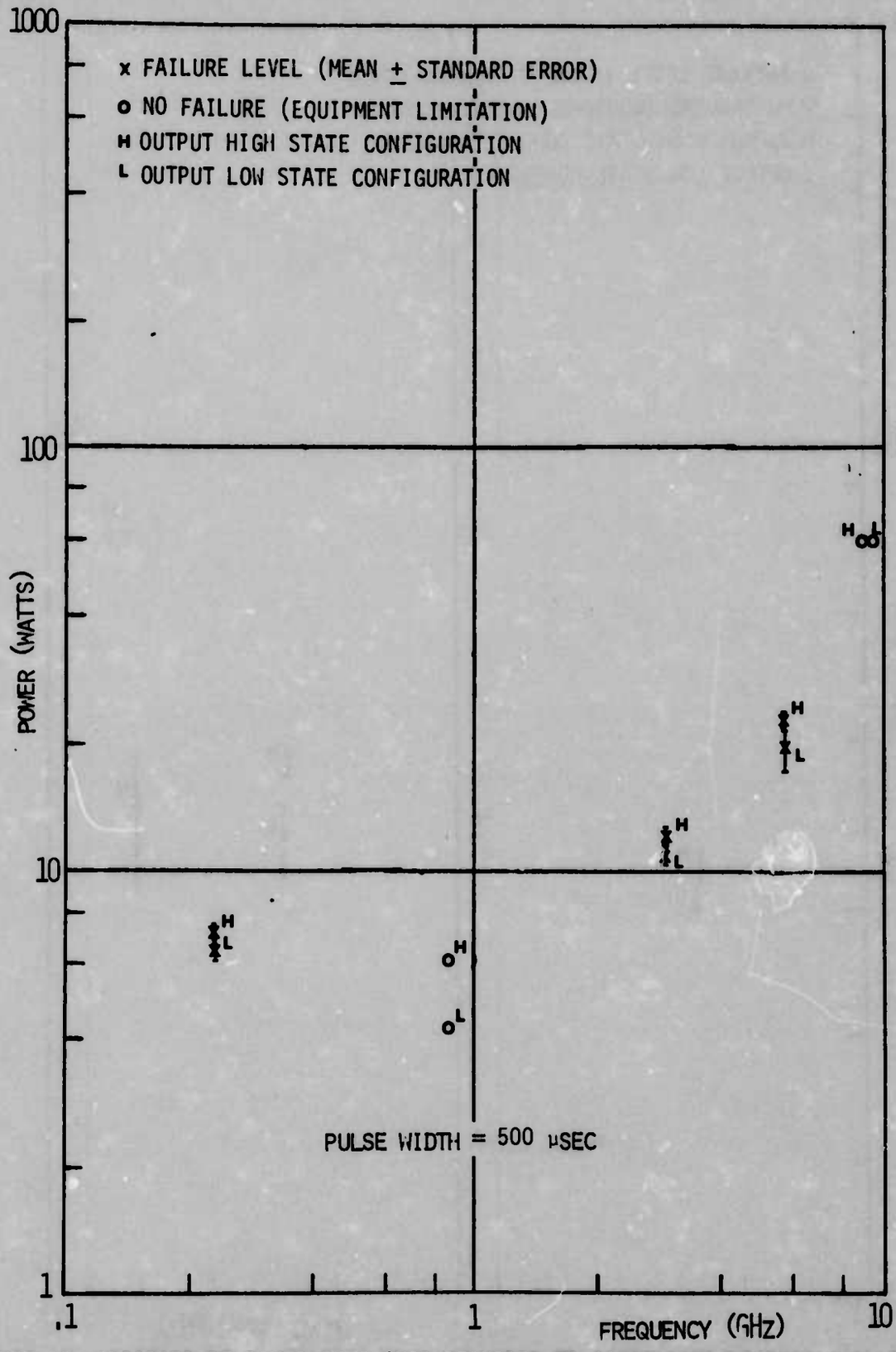


FIGURE 19 ABSORBED RF POWER INTO CHIP REQUIRED TO CAUSE CATASTROPHIC FAILURE AT THE OUTPUT PORT

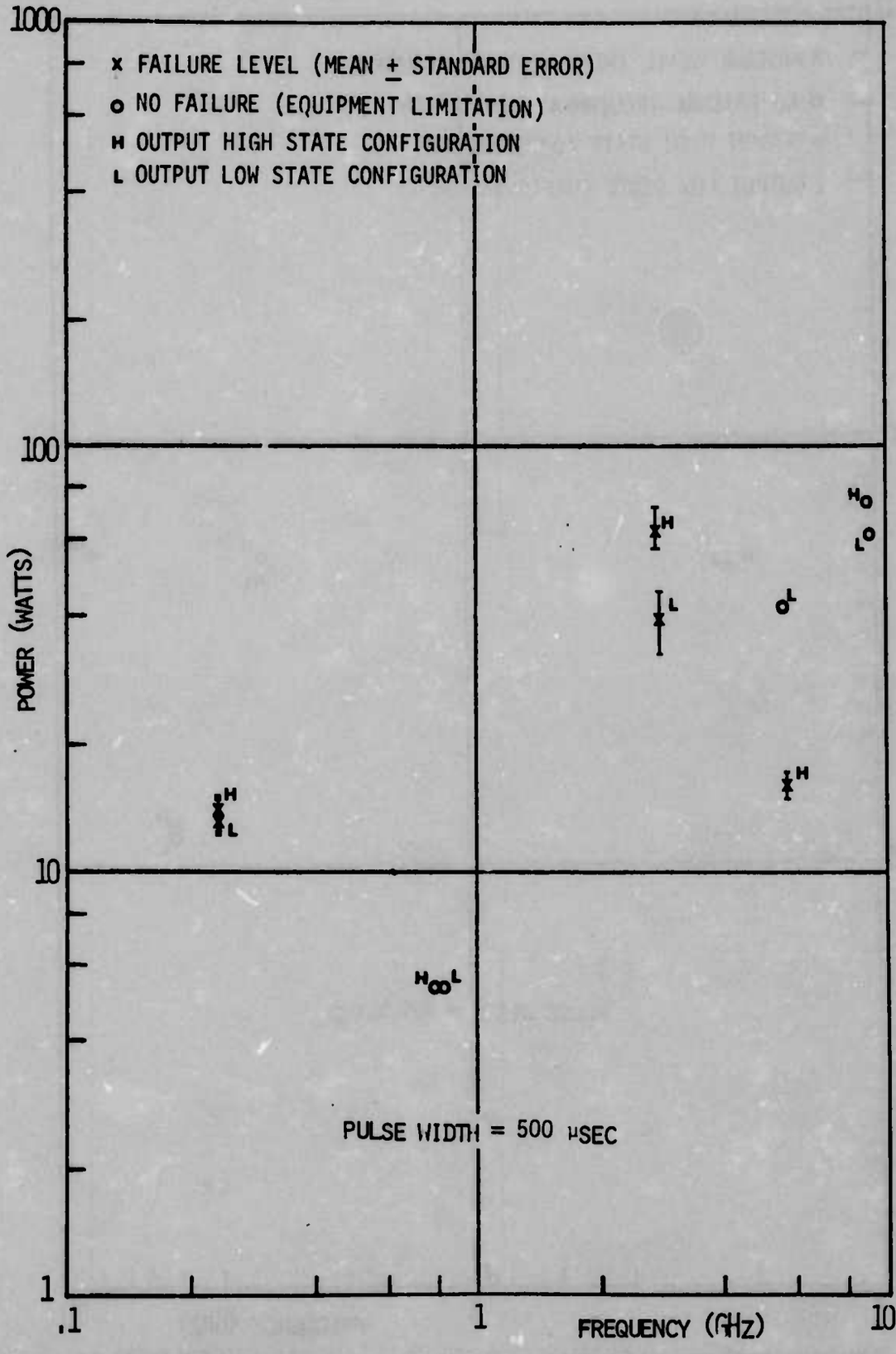


FIGURE 20 ABSORBED RF POWER INTO CHIP REQUIRED TO CAUSE CATASTROPHIC FAILURE AT THE V_{CC} PORT

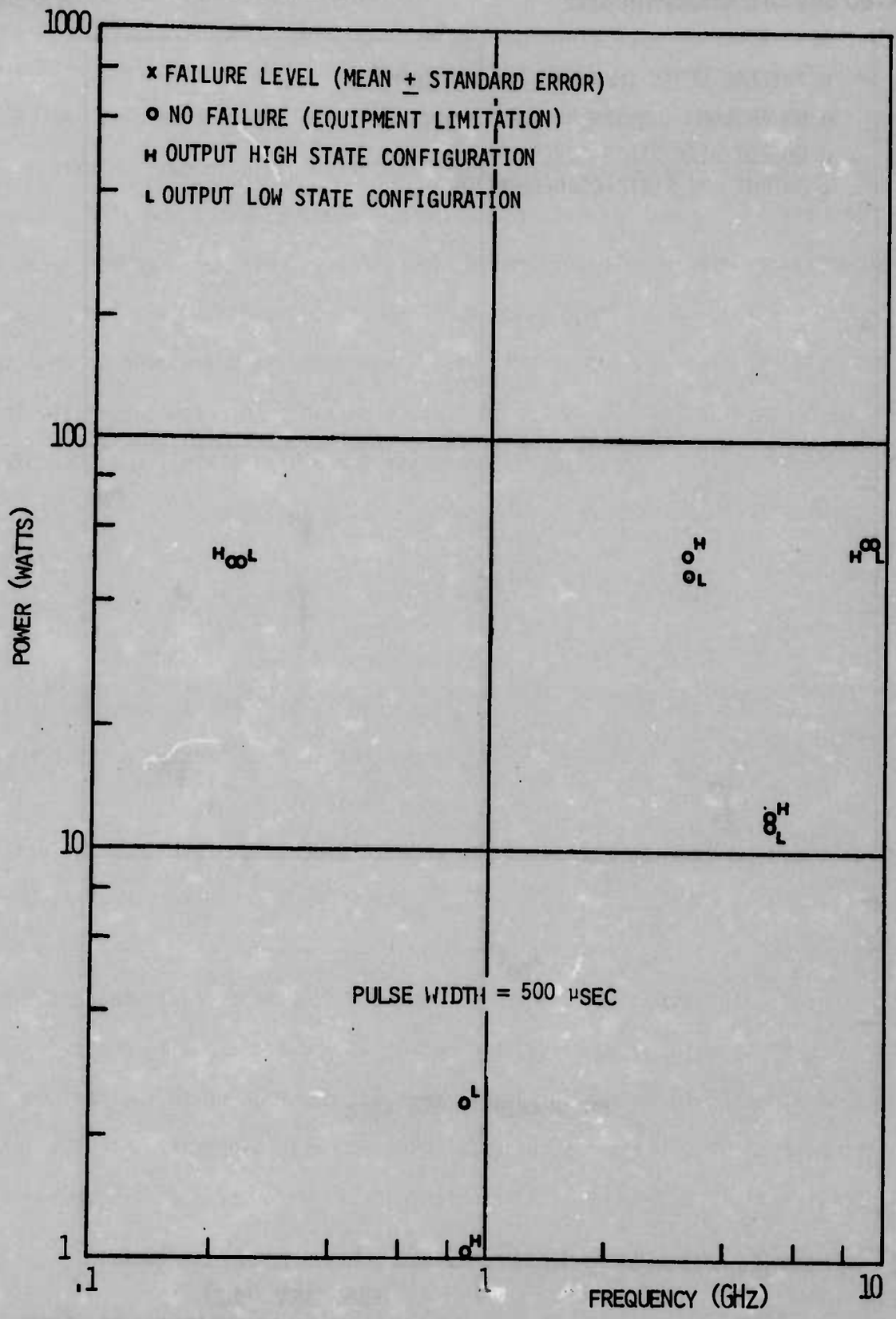


FIGURE 21 ABSORBED RF POWER INTO CHIP REQUIRED TO CAUSE CATASTROPHIC FAILURE AT THE GROUND PORT

Appendix A contains plots of the input and output voltage changes as a function of the observed power for all of the conditions tested in this effort. For purposes of condensing this mass of data into a more comprehendable format, we have chosen arbitrary thresholds and determined the minimum power at which the 7400 crosses thresholds under the influence of the RF drive level. Referring to figure 3, we have chosen 0.8 volts as the maximum value for a low-state condition and 2.0 volts as the minimum value for a high-state condition. These criteria correspond to the guaranteed limits of the manufacturer. It is, of course, possible to choose other limits (e.g., 0.4 volts for a low-state and 2.4 volts for a high-state), and the inferred results would be correspondingly different.

Table 2 displays the results of this analysis. Several useful conclusions can be drawn from a brief study of this table. First, we notice that nearly 70% of the cases tested were not susceptible up to the limit of power (+30 dBm) available in the automatic measurement system. This fact is useful for planning future activities as well as focussing attention on the more susceptible cases. Next, we see a marked frequency dependence as noted previously (see table 3).

Table 2 shows the minimum power required to produce the arbitrary effect chosen for any of the 10 devices that make up the sample for each test condition. There was, of course, a device-to-device spread that varies from quite small to quite large in some cases. In fact, the data group from which the most sensitive case (shown in table 2, RF injected on the output - output low) was drawn also contains one example of a device for which no interference was observed up to the maximum injected power. This type of occurrence is potentially significant to the selection of less susceptible components. A graphical illustration of the failure and interference threshold is shown in figure 22.

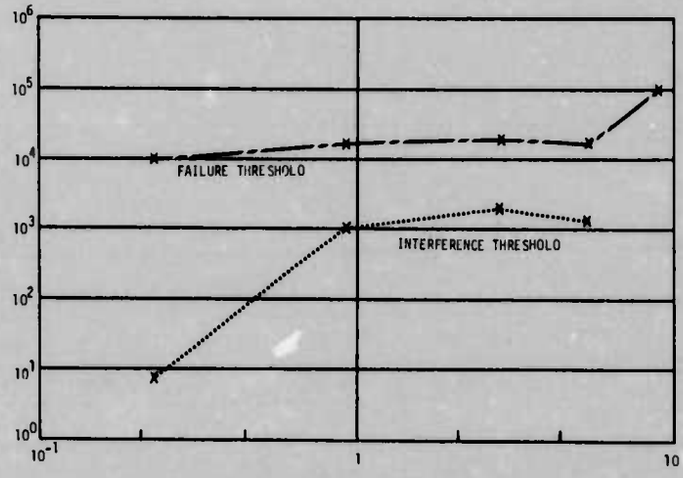
TABLE 2 SUMMARY OF 7400 INTERFERENCE THRESHOLDS

RF INJECTION PORT	OUTPUT BIAS STATE	TEST FREQUENCY				
		0.22 GHz	0.91 GHz	3.0 GHz	5.6 GHz	9.1 GHz
INPUT	HIGH	9 dBm	30 dBm	31 dBm	33 dBm	31 dBm
	LOW	*	*	*	*	*
OUTPUT	HIGH	~25 dBm	~28 dBm	~30 dBm	*	*
	LOW	6 dBm	10 dBm	19 dBm	*	*
V_{cc}	HIGH	*	*	*	*	*
	LOW	21 dBm	*	*	*	*
GROUND	HIGH	19 dBm	*	*	*	*
	LOW	13 dBm	*	*	*	*

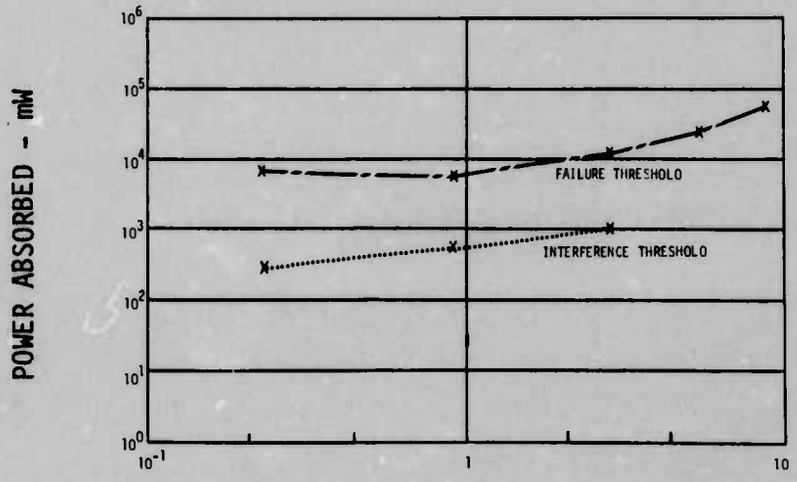
~ - RESULT EXTRAPOLATED FROM DATA
* - THRESHOLD NOT CROSSED UP TO LIMIT OF + 30 dBM ABSORBED IN DEVICE
INTERFERENCE CRITERIA: OUTPUT HIGH STATE - OUTPUT DROPS BELOW 2.0 VOLTS
OUTPUT LOW STATE - OUTPUT INCREASES ABOVE 0.8 VOLTS

TABLE 3 SUMMARY OF 7400 FREQUENCY DEPENDENCE

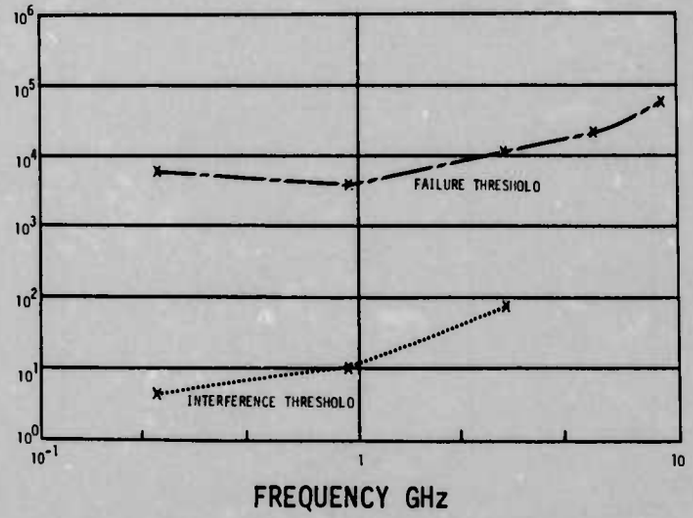
FREQUENCY (GHz)	% OF CASES SUSCEPTIBLE TO RF POWER
0.22	75.0
0.91	37.5
3.00	37.5
5.60	12.5
9.10	12.5



(A) RF INJECTED INTO INPUT - OUTPUT HIGH BIAS STATE



(B) RF INJECTED INTO OUTPUT - OUTPUT HIGH BIAS STATE



(C) RF INJECTED INTO OUTPUT - OUTPUT LOW BIAS STATE

FIGURE 22 7400 SUSCEPTIBILITY DATA SUMMARY

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3. THEORY OF RF EFFECTS IN BIPOLAR DEVICES

Analysis of the 7400 NAND gate interference data indicates that the fundamental susceptibility effect is rectification. In order to substantiate this observation, we will discuss how this rectification can be accounted for, its functional dependence on RF power and frequency, and make several circuit implications to justify its existence.

3.1 Rectification - In order to accurately describe the various observed interference effects of the 7400, we must recognize that all pn junctions contained on the chip become possible sites for rectification. Furthermore, these pn junctions can be divided into two categories. The first group is referred to as functional circuit pn junctions, and the second group as parasitic pn junctions. Functional junctions are those which are used to perform the actual circuit operation. As an example, all of the pn junctions indicated in the schematic diagram (figure 1) of the 7400 are classed as functional circuit pn junctions, since they are used in the actual signal processing.

On the other hand, parasitic pn junctions are those which exist on the chip by virtue of the process used to make these integrated circuits, but perform no direct function in the circuit operation. Examples of how various parasitic junctions arise in the manufacture of integrated circuits are illustrated in figure 23. A schematic diagram showing the parasitic junctions present in the 7400 is shown in figure 24.

Rectification in pn junctions arises from the nonlinearity of the junction, and is a well-treated subject in the literature [4, 5] so we will not go into great detail here. Figure 25 shows a model of a pn junction which is adequately treated by the familiar diode equation

$$I_j = I_o \left(e^{qV_j/kT} - 1\right) \qquad (1)$$

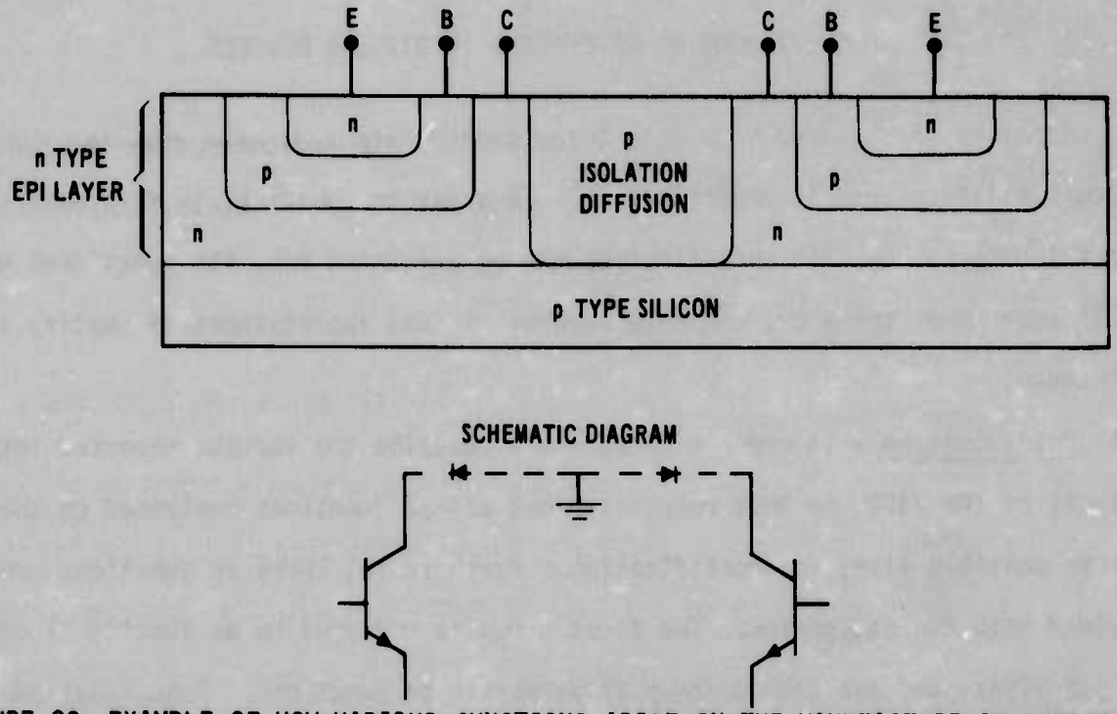

FIGURE 23 EXAMPLE OF HOW VARIOUS JUNCTIONS ARISE IN THE MANUFACTURE OF INTEGRATED CIRCUITS

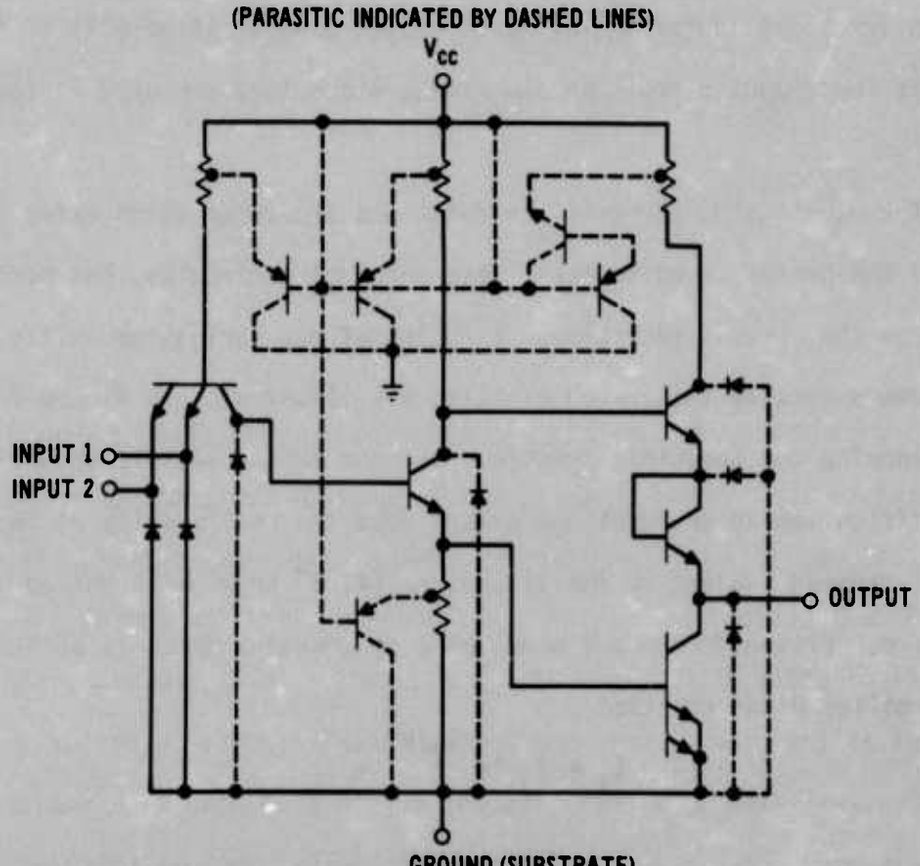

FIGURE 24 PARASITIC DIAGRAM OF THE 7400

where:

I_j = junction current

I_o = constant depending upon junction

V_j = junction voltage

q = electron charge

T = temperature (°K)

k = Boltzman's constant.

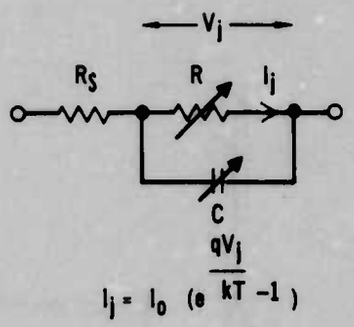

FIGURE 25 PN DIODE MODEL

When an RF signal is impressed across the junction, an average current is generated which can be modelled by a Norton or Thevenin equivalent circuit as shown in figure 26. The value of the current generator (or voltage source) and R_g are both functions of the RF drive level. For small drive levels, the rectified current is proportional to the absorbed RF power (square law detection) so that,

$$I_g = \eta P_{RF} \text{ (absorbed)} \qquad (2)$$

where η = rectification efficiency [mA/mW]. The rectification efficiency can be derived, and is found to have a frequency dependent term and a constant term.

$$\eta = \underbrace{\frac{q/kT}{(1 + r_s/R^2)}}_{\eta_o} \cdot \underbrace{\frac{1}{1 + \frac{\omega^2 C^2 r_s R^2}{R + r_s}}}_{\text{FREQUENCY DEPENDENT TERM}} \qquad (3)$$

Figure 27 is a generalized plot of the rectification efficiency versus frequency. The breakpoint of the curve depends upon the junction capacitance and resistance, and can probably be related to switching speed or frequency cutoff. As will be seen later, the 7400 junctions operate on the sloping part of the curve.

In usual practice, the values of I_g, R_g, and η are determined empirically through a measurement of the open circuit voltage and short circuit current developed at a series of RF power levels. Since it is not possible to make such measurements on the junction buried deep inside an IC chip, the values must be inferred from other measurements.

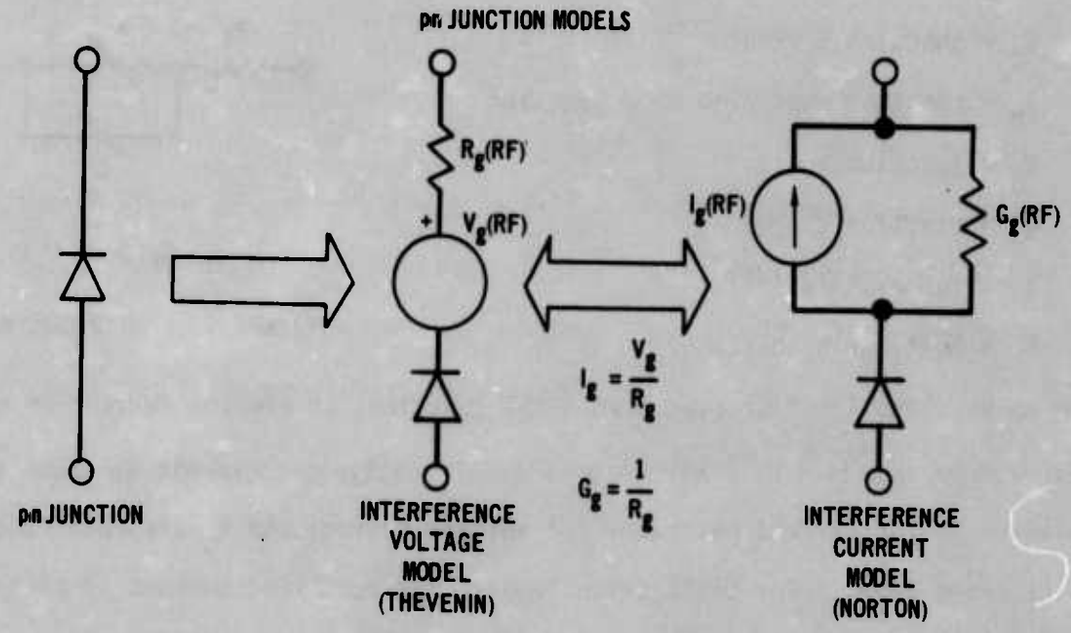

FIGURE 26 NORTON AND THEVENIN EQUIVALENT CIRCUITS USED TO REPRESENT A PN JUNCTION UNDER THE INFLUENCE OF RF ENERGY

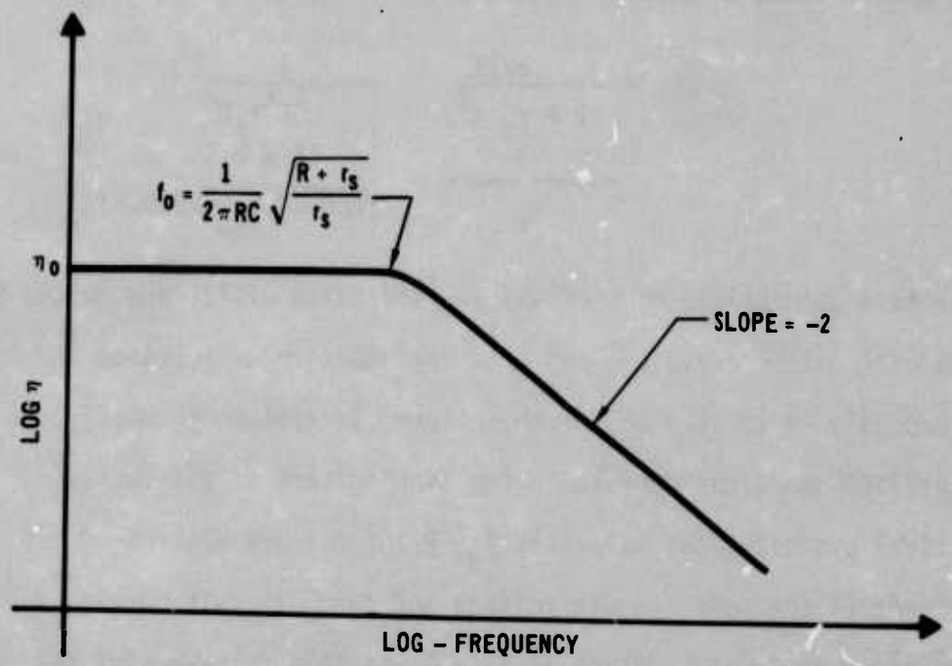

FIGURE 27 PROPERTIES OF RECTIFICATION EFFICIENCY

In general, we expect those junctions which are directly across external terminals to be driven much harder than interior junctions which are decoupled from the RF signal by both series and parallel elements along the RF path. Accordingly, RF effects in the chip can be divided into first order and higher order effects depending upon how much decoupling takes place (that is to imply that the effect is reduced at a given power input level). Most of the analysis to follow will be concerned with first order effects, but it should be remembered that the reduction or elimination of these effects (perhaps in another manufacturer's chip) will bring the higher order effects to the fore.

3.2 Interference Generators in the 7400 NAND Gate - Now that we have discussed how to characterize the RF response of a pn junction, we must determine where the rectification is most likely to occur for a specific RF entry port. In the next two sections, the primary interference generators at the input and output of the 7400 will be identified.

3.2.1 RF Entering the Input - Consider the case of RF entering the input with the input low. By examination of figure 28 we see that the clamping diode located at the input of the device directly shunts the RF source. Therefore, this diode becomes a very likely candidate for rectification. Also by examination of the interference data (shown in figure 9), we see that an excessive amount of current is flowing out of the input of the device, approximately 9 mA above its DC value. These data support the argument that rectification is indeed occurring at the clamping diode.

This case also exhibits an interesting higher order effect. It will be recalled (section 2.1.2.1) that a complete output state change was observed under these conditions. Since the input voltage increased with the RF drive it would be expected for the output to change as a normal circuit response to the increased input voltage. That this is not happening is illustrated in figure 29 where the corresponding input and output voltage are plotted along with the normal input-output relationship. Evidently, the RF signal is coupled across transistor T1 and rectified in the

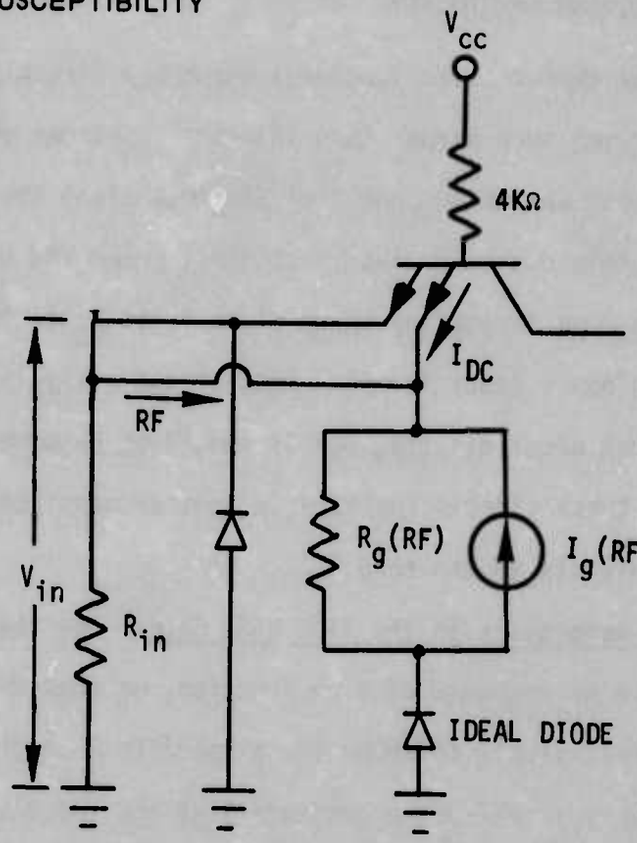

FIGURE 28 LOCATION OF PRIMARY INTERFERENCE GENERATOR FOR RF ENTERING THE INPUT

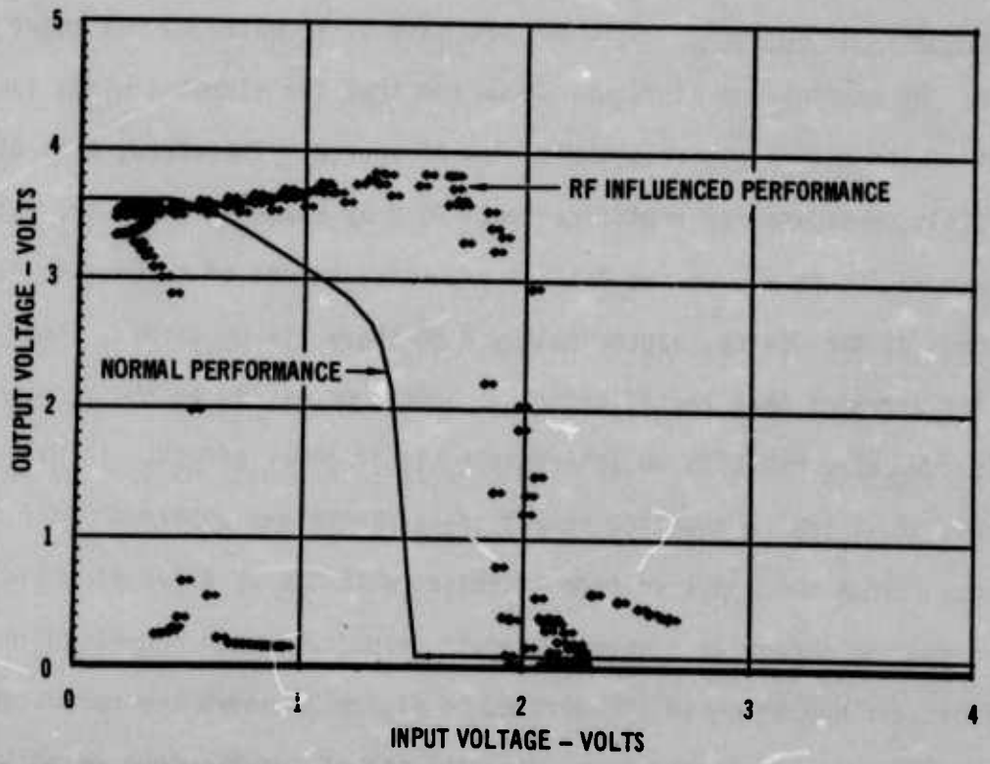

FIGURE 29 COMPARISON OF INPUT AND OUTPUT CHARACTERISTICS, OUTPUT HIGH - INPUT LOW BIAS STATE, FREQUENCY - 0.22 GHz

collector isolation diode. The rectified current then drives T2 into conduction which ultimately leads to a change-of-state at the output. Figure 30 shows the inferred interference generators on the input.

3.2.2 RF Entering the Output - Referring to the parasitic diagrams of the 7400 (figure 24), we see that a parasitic diode directly shunts output transistor T4. Therefore, this diode becomes an ideal site for rectification. Further investigation of the output indicates that, depending upon the external bias arrangement, other parasitic diodes can contribute to the RF response. Figure 31 indicates all possible rectification sites that appear at the output.

For the output low case, the principle RF generator is the parasitic diode which shunts transistor T4. This generator is illustrated in figure 32. For the output high case, the principle RF generator is D3 which is in series with the output. This generator is shown in figure 33. Note that we have chosen to represent the series generator as a Thevenin source.

3.3 Manifestation of Interference - Thus far, we have shown that rectification is the primary interference effect, where it can occur, and how it can be modelled. We have also postulated where the primary rectification sites exist. The problem now is how to use the above information to predict the overall response of the circuit. The answer is that substituting the interference generators for their respective circuit elements and using normal circuit analysis, the response can be calculated. For example, the input voltage can be calculated by replacing the clamping diode with its Norton equivalent and writing the correct loop equations for the input voltage. This will be described in the next section.

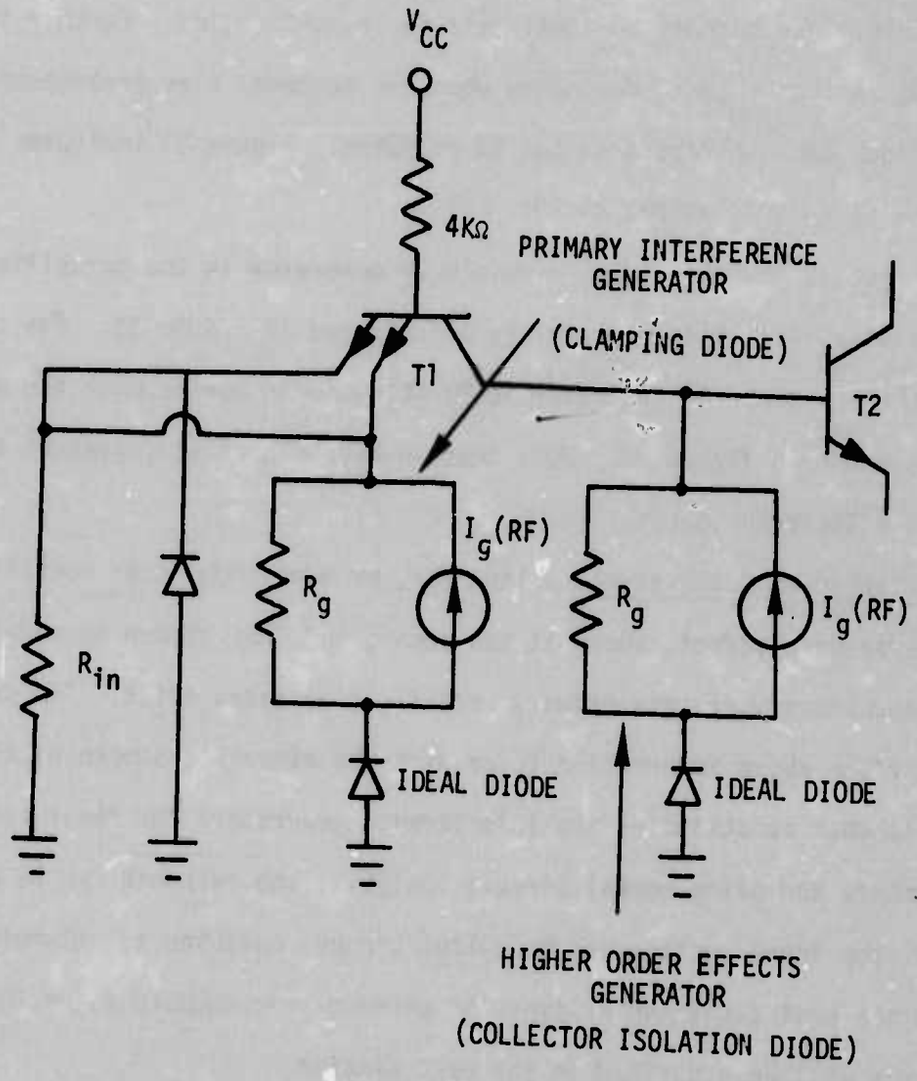

FIGURE 30 SUMMARY OF IMPLIED INTERFERENCE GENERATORS FOR RF ENTERING THE INPUT

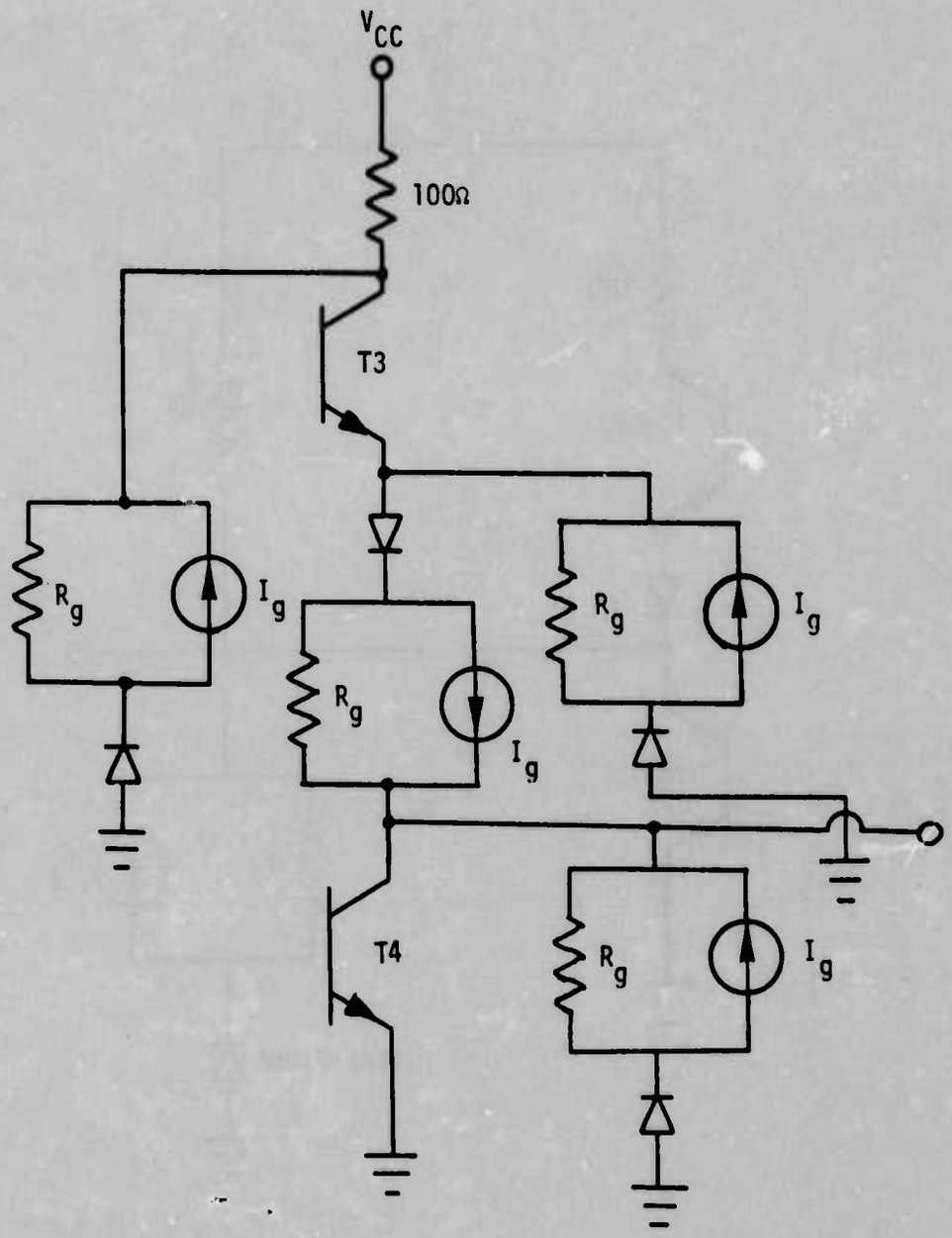

FIGURE 31 POSSIBLE RECTIFICATION SITES APPEARING AT THE OUTPUT

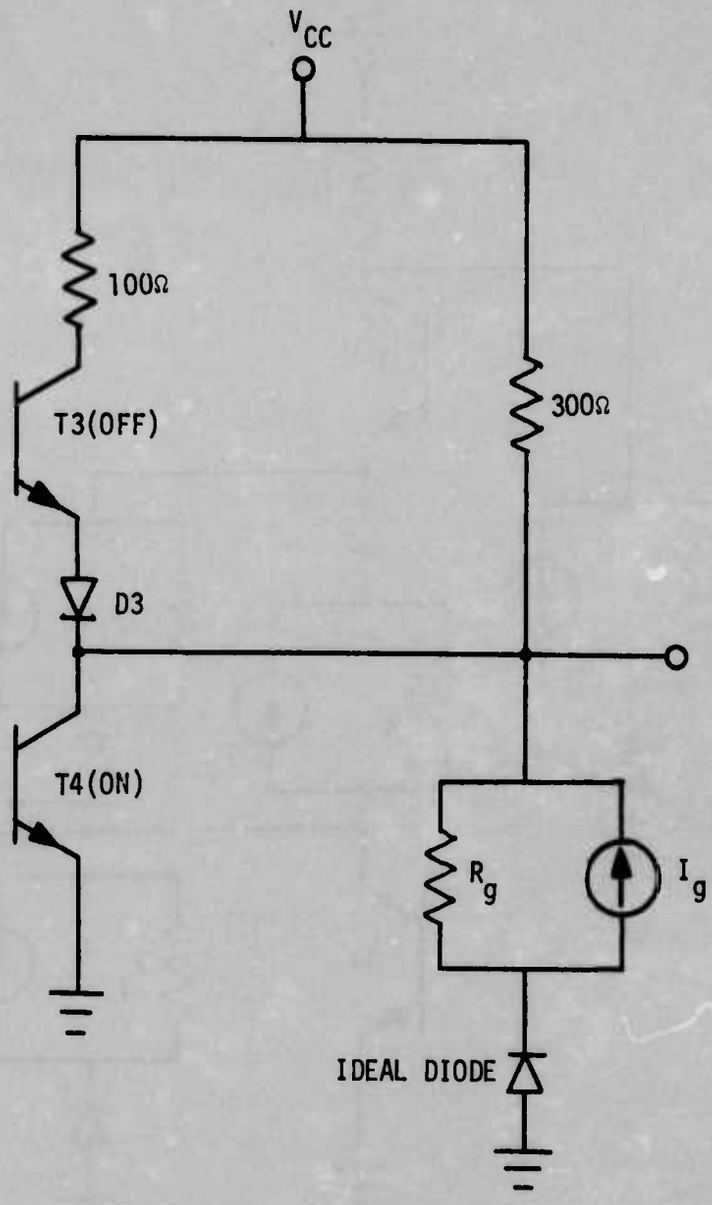

FIGURE 32 PRIMARY INTERFERENCE GENERATOR FOR RF ENTERING OUTPUT - OUTPUT LOW CASE

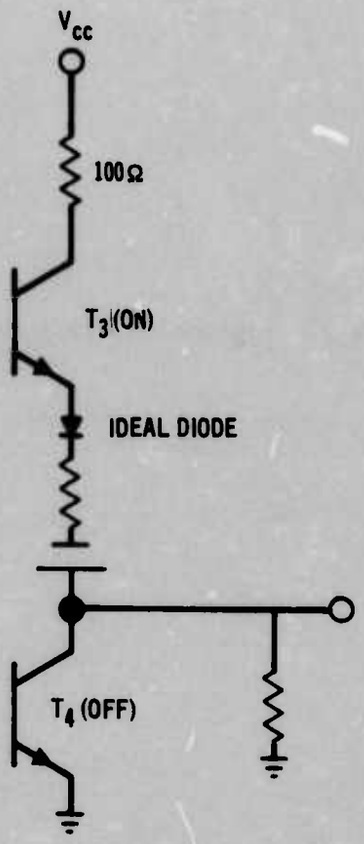

FIGURE 33 PRIMARY INTERFERENCE GENERATOR FOR RF ENTERING THE OUTPUT - OUTPUT HIGH CASE

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4. ANALYSIS OF RF EFFECTS AND MODEL DEVELOPMENT

In this section, a method will be discussed as to how the generator frequency and power dependence can be determined and, how the generator can be used to predict the interference. In addition, several comparisons of the predicted and actual interference data will be made.

4.1 Characterization of Interference Generators - Ideally, all that is required to define a Norton or Thevenin generator is the open circuit voltage and short circuit current measured at the terminals of the device. Since the interference generators we are dealing with have dependence upon RF power and frequency, the open circuit and short circuit measurements must be made at a particular RF power and frequency level. Before we present a specific example of how the RF power and frequency dependence of a particular generator is calculated, a few remarks are in order.

It should be noted that the measured values of open circuit voltage and short circuit current are probably due to the contribution from several pn junctions. However, as a first order approximation to the RF performance of the device, the interference generator derived from these lumped measurements can be used to replace the pn junction which was inferred in section 3.2 as the primary cause for the observed interference. Comparisons of the measured interference with that predicted by the derived interference generators will serve to substantiate the models and assumptions. The particulars used to define the RF power and frequency dependence of a Norton or Thevenin interference generator are discussed below.

As an example, we will discuss how the dependence of the generator used to represent the input clamping diode is calculated. In order to define the RF power dependence of this diode, the open circuit voltage and short circuit current measured across its terminals at several different RF power levels at a constant frequency are required. For ease of measurement, the voltage across a 10 ohm loading resistor was used in lieu of the short circuit current. A plot of the open circuit

voltage and the voltage across the 10 ohm loading resistor measured at an RF frequency of 0.22 GHz is shown in figures 34 and 35, respectively. The current through the resistor can be calculated using Ohm's Law. Table 4 summarizes the values taken from these plots at 20 different power levels. From the data in this table, the Norton or Thevenin generator resistance (R_g) at a particular power and frequency can be calculated using the following equation:

$$R_g = \frac{V_{oc} - V_{10}}{I_{10}} \tag{4}$$

where V_{oc} is the open circuit voltage, V_{10} is the voltage across the 10 ohm loading resistor, and I_{10} is the current through the 10 ohm resistor. Next, the short circuit current (I_g) of the Norton generator is calculated using

$$I_g = \frac{V_{oc}}{R_g} \tag{5}$$

Finally, the value of the Thevenin voltage generator is simply the open circuit voltage at the given power level. As a sample calculation, R_g, I_g, and V_g are calculated at an RF power level of 100 mW and frequency of 0.22 GHz.

$$R_g = \frac{V_{oc} - V_{10}}{I_{10}} = \frac{3.29V - 0.183V}{18.28\ mA} = 170\Omega$$

$$I_g = \frac{V_{oc}}{R_g} = \frac{3.29V}{.17K\Omega} = 19.35\ mA$$

$$V_g = V_{oc} = 3.29V$$

Table 5 lists the characteristics of the interference generators representing the clamping diode for 20 RF power levels (all at a 0.22 GHz frequency).

The frequency dependence of the above generator is found using the same procedure just discussed with the exception that the open circuit voltage and short circuit current were measured at frequencies other than 0.22 GHz. Tables 6 and 7 give the generator characteristics at 0.91 GHz and 3 GHz, respectively.

The same procedure was carried out on the parasitic diode across the output with similar results (discussed below). It is instructive to study the rectification

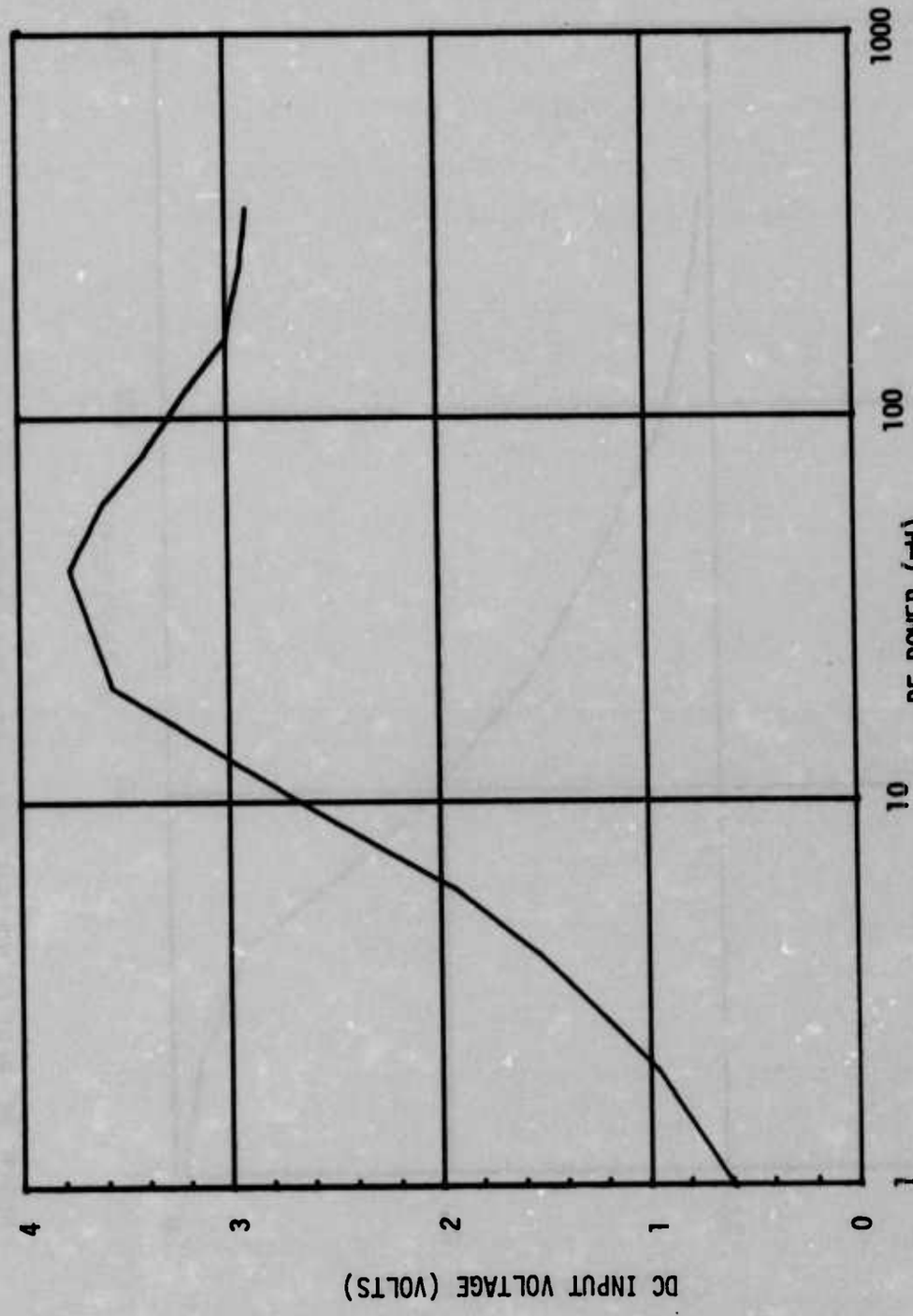


FIGURE 34 PLOT OF OPEN CIRCUIT VOLTAGE VS RF POWER ACROSS THE INPUT DIODE FOR 0.22 GHz (NO BIAS CONDITIONS)

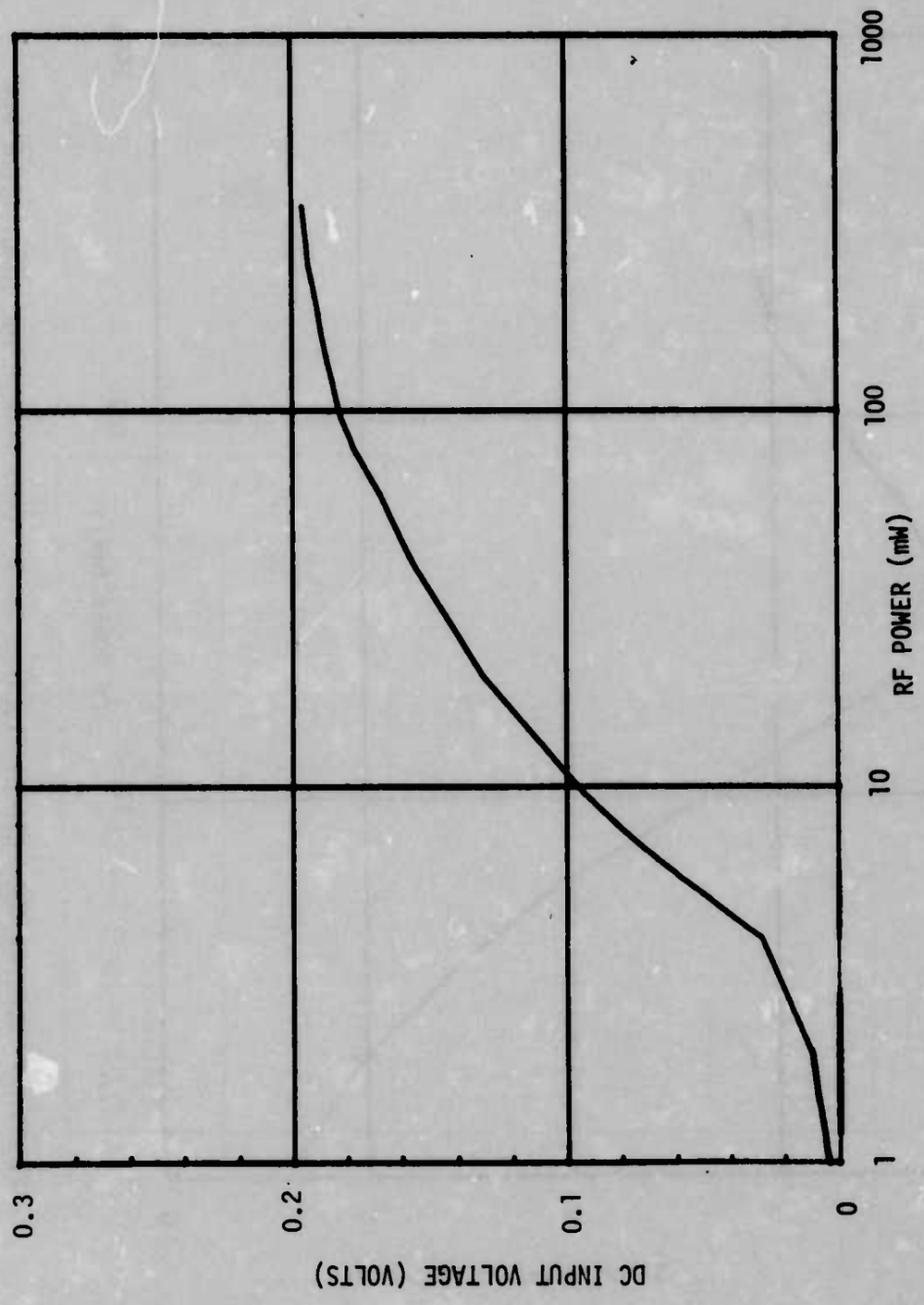


FIGURE 35 PLOT OF VOLTAGE ACROSS 10 OHM LOADING RESISTOR VS RF POWER FOR THE INPUT DIODE FOR 0.22 GHz (NO BIAS CONDITIONS)

TABLE 4 MEASURED VALUES OF VOLTAGE AND CURRENT FOR THE INPUT DIODE AT A FREQUENCY OF 0.22 GHz (NO BIAS CONDITIONS)

POWER (mW)	R = OPEN CIRCUIT		R = 10Ω	
	V_{in} (V)	I_{in} (mA)	V_{in} (V)	I_{in} (mA)
1	0.591	0.000	0.004	0.40
2	0.960	0.000	0.011	1.05
4	1.521	0.000	0.028	2.82
6	1.934	0.000	0.061	6.08
8	2.344	0.000	0.082	8.17
10	2.654	0.000	0.096	9.56
20	3.569	0.000	0.131	13.13
40	3.765	0.000	0.156	15.61
60	3.601	0.000	0.167	16.74
80	3.413	0.000	0.177	17.72
100	3.290	0.000	0.183	18.28
120	3.189	0.000	0.185	18.52
140	3.087	0.000	0.188	18.76
160	3.002	0.000	0.189	18.93
180	2.983	0.000	0.190	19.04
200	2.965	0.000	0.192	19.16
240	2.929	0.000	0.194	19.38
260	2.920	0.000	0.195	19.47
300	2.908	0.000	0.195	19.54
350	2.893	0.000	0.196	19.64

TABLE 5 INPUT DIODE GENERATOR CHARACTERISTICS FOR 0.22 GHz

POWER ABSORBED (mW)	Rg (Ω)	Vg (V)	Ig (mA)
1.00	1475	0.591	0.40
2.00	903	0.960	1.06
4.00	530	1.521	2.87
6.00	308	1.934	6.28
8.00	277	2.344	8.47
10.00	267	2.654	9.92
20.00	262	3.569	13.63
40.00	231	3.765	16.29
60.00	205	3.601	17.56
80.00	183	3.413	18.69
100.00	170	3.290	19.35
120.00	162	3.189	19.66
140.00	155	3.087	19.97
160.00	149	3.002	20.20
180.00	147	2.983	20.34
200.00	145	2.965	20.48
240.00	141	2.929	20.75
260.00	140	2.920	20.86
300.00	139	2.908	20.95
350.00	137	2.893	21.07

TABLE 6 INPUT DIODE GENERATOR CHARACTERISTICS FOR 0.91 GHZ

POWER ABSORBED (mW)	Rg (Ω)	Vg (V)	Ig (mA)
1.00	18283	0.207	0.01
2.00	10932	0.461	0.04
4.00	7250	0.906	0.13
6.00	6031	1.335	0.22
8.00	4985	1.601	0.32
10.0	4673	2.037	0.44
20.00	2640	2.611	0.99
40.00	1806	3.338	1.85
60.00	1328	3.397	2.56
80.00	1031	3.348	3.25
100.00	874	3.300	3.78
120.00	759	3.251	4.28
140.00	668	3.202	4.79
160.00	595	3.152	5.30
180.00	534	3.103	5.81
200.00	487	3.058	6.28
240.00	430	2.990	6.95
260.00	406	2.959	7.28
300.00	358	2.893	8.10
350.00	275	2.820	10.25

TABLE 7 INPUT DIODE GENERATOR CHARACTERISTICS FOR 3.0 GHz

POWER ABSORBED (mW)	Rg (Ω)	Vg (V)	Ig (mA)
2.00	400000	0.557	0.00
3.00	64747	0.828	0.01
4.00	33144	0.988	0.03
6.00	19033	1.291	0.07
8.00	13598	1.479	0.11
10.00	9797	1.498	0.15
20.00	4300	1.608	0.37
40.00	2822	2.101	0.74
60.00	2091	2.244	1.07
80.00	1742	2.369	1.36
100.00	1487	2.401	1.61
120.00	1278	2.335	1.83
140.00	1113	2.269	2.04
160.00	993	2.209	2.23
180.00	921	2.201	2.39
200.00	866	2.205	2.55
240.00	781	2.213	2.83
260.00	750	2.213	2.95
300.00	693	2.199	3.17
350.00	637	2.179	3.42

efficiency of these two pn junctions. Figure 36 shows the measured rectification efficiencies (in the square law region) plotted against frequency. As can be seen, the junctions are operating on the sloping part of the rectification efficiency prediction curve, and this undoubtedly explains the frequency dependence of the interference effects described earlier.

4.2 Circuit Implications in the 7400 NAND Gate - As a check on the validity of our assumptions, we examined the test cases discussed in section 2, and will present possible explanations for the RF effects and show that, by using the model derived above, we can predict, to some degree of accuracy, the interference effects. We will also consider some typical interconnection with other TTL gates and discuss what RF effects might occur based upon our present model.

4.2.1 RF Entering the Input With the Input Low - As discussed in section 3.2.1, the clamping diode located at the input was identified as the primary interference generator for RF entering the input. The characteristics of this generator were calculated (using the methods presented in section 4.1) and are displayed in figures 37 and 38.

In order to make a comparison, consider the test setup that was used to collect the interference data for this case. Figure 39 shows the setup with the Norton interference generator representing the clamping diode. Analytically, the input voltage can be expressed by

$$V_{in} = (I_{DC} + I_g)/(1/R_g + 1/R_{in}) \qquad (6)$$

Note that in equation 6 we have assumed I_{DC} to be a constant value, however, in reality it is a variable and diminishes with increasing input voltage. It should also be noted that equation 6 does not hold if the quantity $I_g \cdot R_g < 0.2$ volts. As an example, equation 6 is used to calculate the implied input voltage at an RF power of 100 mW and a frequency of 0.91 GHz. The values of I_g and R_g were obtained from figures 37 and 38. The value of R_{in} is 200 ohms, and I_{DC} is measured under DC conditions.

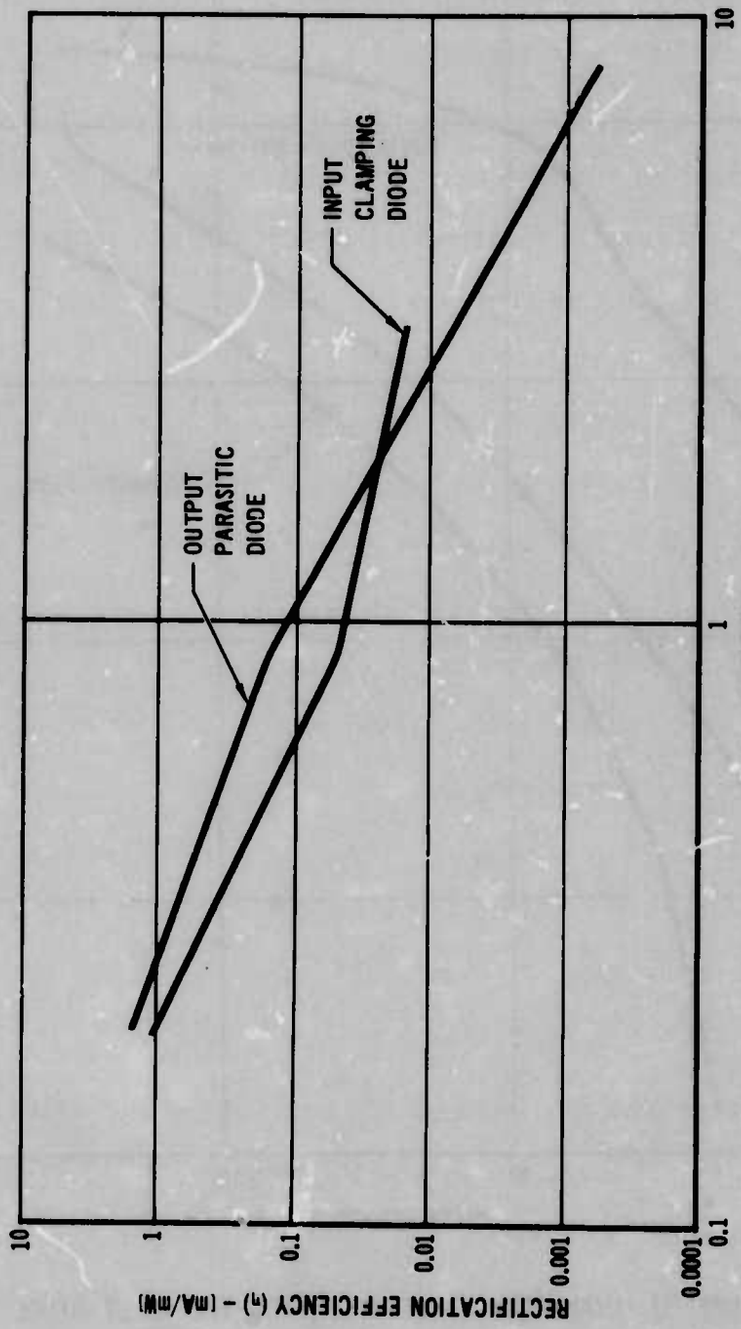


FIGURE 36 MEASURED RECTIFICATION EFFICIENCY

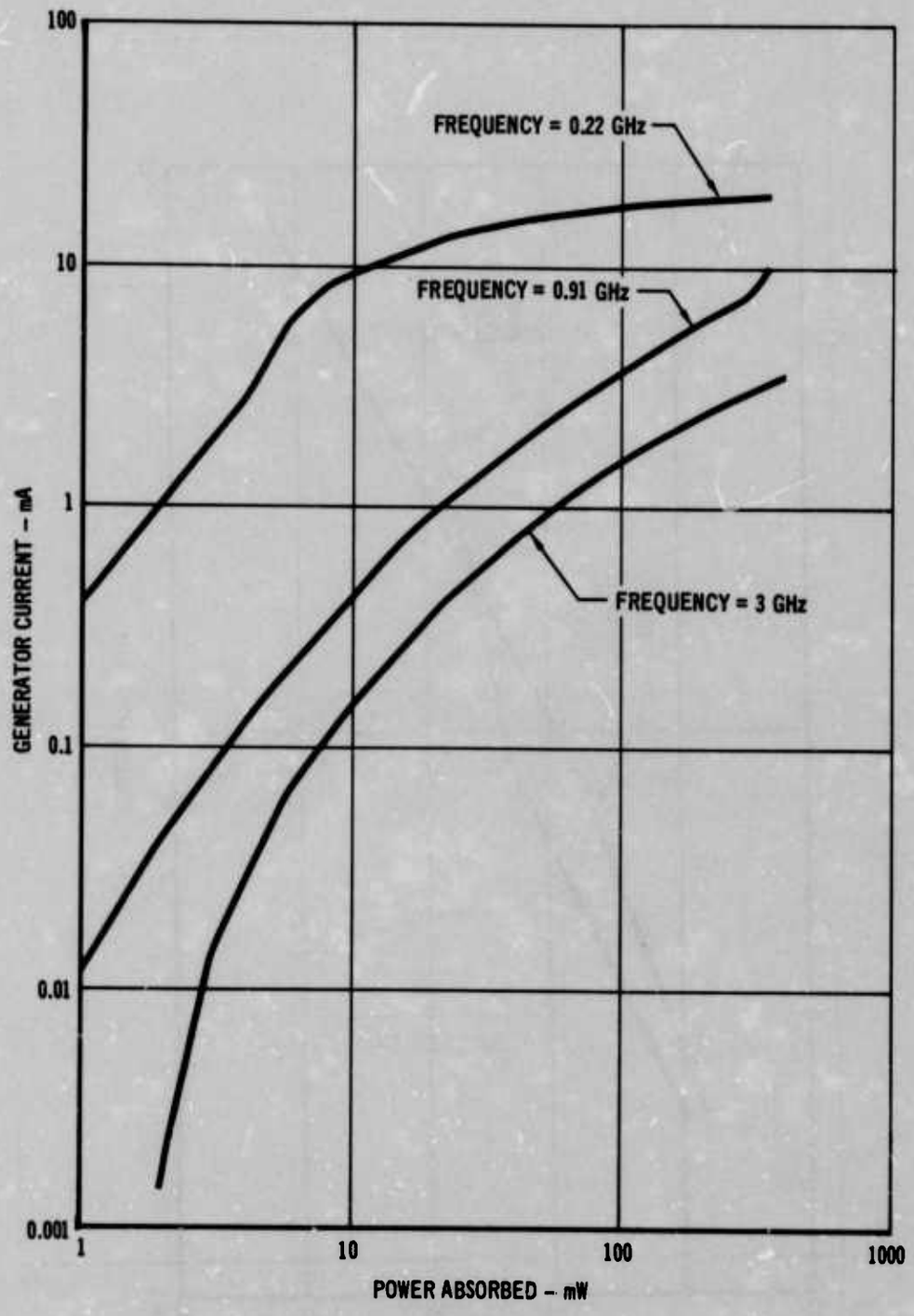


FIGURE 37 CHARACTERISTICS OF I_g FOR THE INPUT DIODE

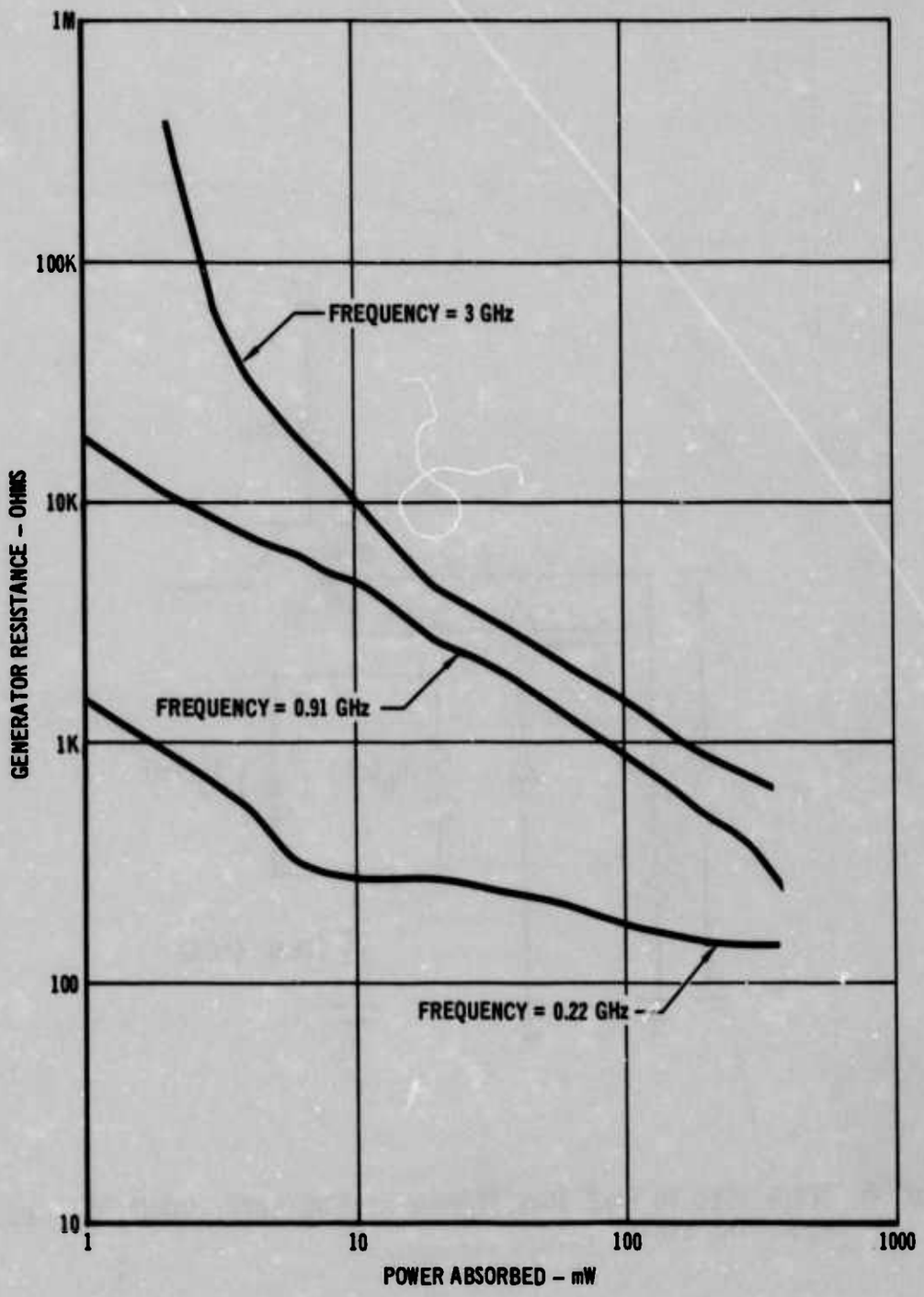


FIGURE 38 CHARACTERISTICS OF R_g FOR THE INPUT DIODE

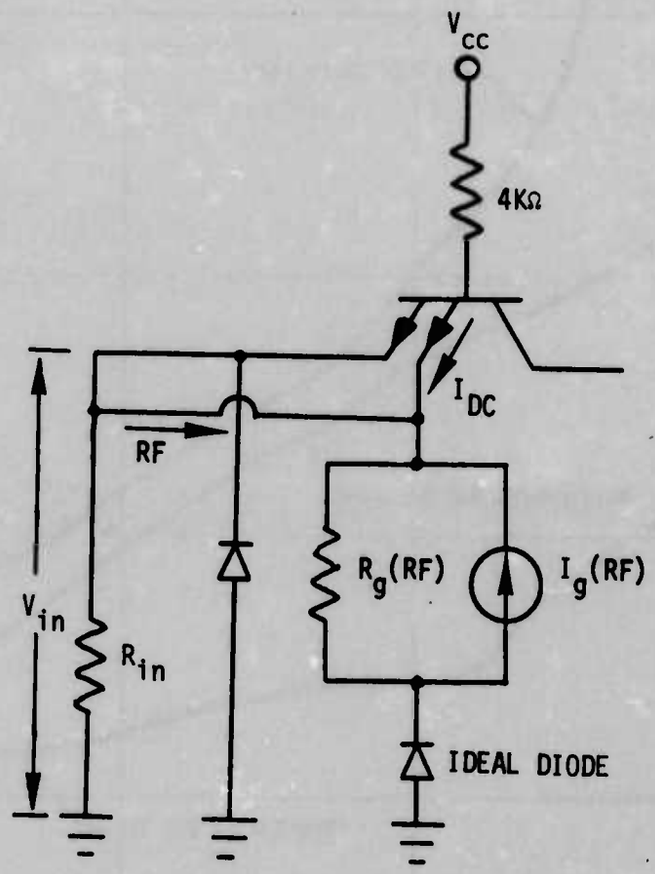


FIGURE 39 SETUP USED TO MAKE INTERFERENCE MEASUREMENTS, INPUT LOW - OUTPUT HIGH BIAS STATE

$$V_{in} = (I_{DC} + I_g)/(1/R_g + 1/R_{in})$$

$$V_{in} = (0.8\ mA + 3.78\ mA)/(1/0.874K\Omega + 1/0.2K\Omega) = 0.74V$$

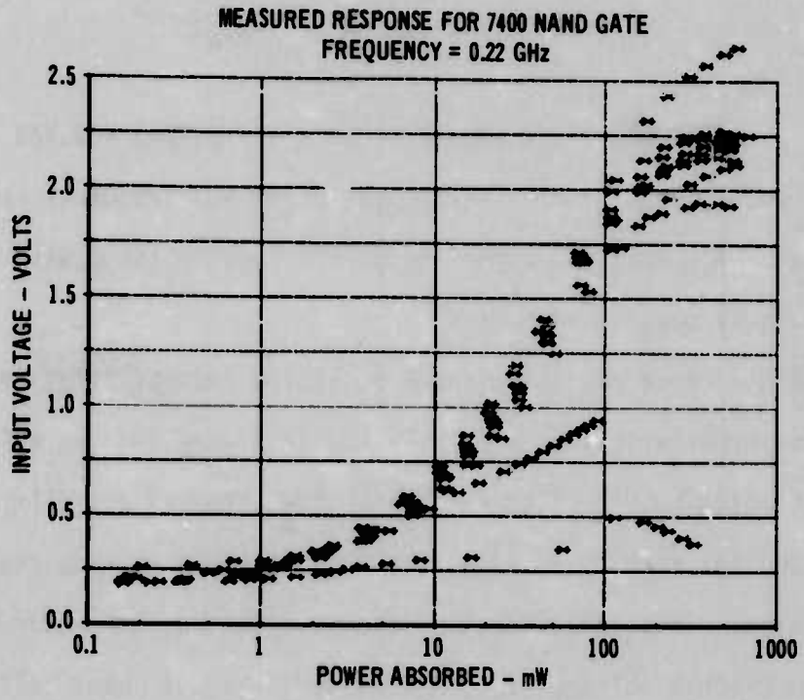
The implied input current at this particular power and frequency can be calculated using Ohm's Law. A graphical comparison of the input voltage with the interference data is shown in figures 40 through 42.

The problem of more realistic interconnection possibilities can be handled by considering the hypothetical case illustrated in figure 43. We will assume that gate 1 is unaffected by RF. Figure 44 shows the internal circuitry of gates 1 and 2 that is needed for this discussion. It must be borne in mind that this is a nonlinear problem. Thus, the effect of the interference generator will not appear until its open circuit voltage ($I_g \cdot R_g$) exceeds the quiescent voltage already present. After that point, the interference generator will dominate and the implied input voltage can be expressed by

$$V_{in} = V_{ce} = (I_{DC} + I_g - I_c)R_g \qquad (7)$$

Therefore, to solve equation 7 the characteristics of transistor T4 are required.

To continue the discussion of this problem, a graphical solution to equation 7 is indicated in figure 45 for an arbitrary RF power level. From figure 45 and equation 7 it can be seen that the value of V_{in} (and I_{in}) of gate 2, is dependent upon I_{DC}, I_g, R_g and the characteristics of transistor T4. It can also be seen from this figure that in order for the input of gate 2 to remain in the low state, the operating point must stay in the saturation region of the transistor characteristics. Now, as I_g increases for an increase of RF power, the load line shifts to the right as shown in figure 46. If the change is large enough, the input will go high and change the state of the output of gate 2.



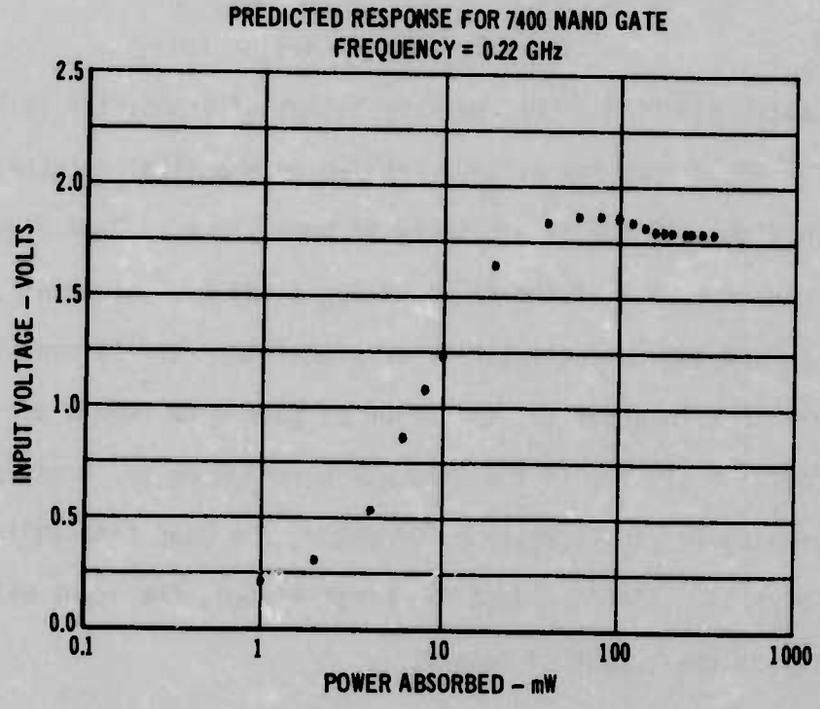
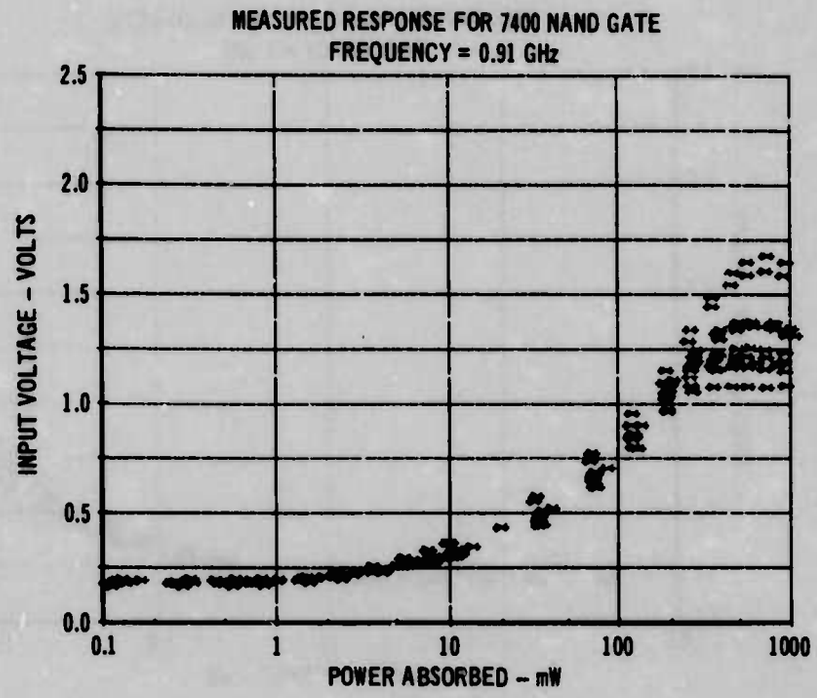


FIGURE 40 COMPARISON OF PREDICTED AND ACTUAL INTERFERENCE DATA FOR RF ENTERING THE INPUT, INPUT LOW BIAS STATE (0.22 GHz)



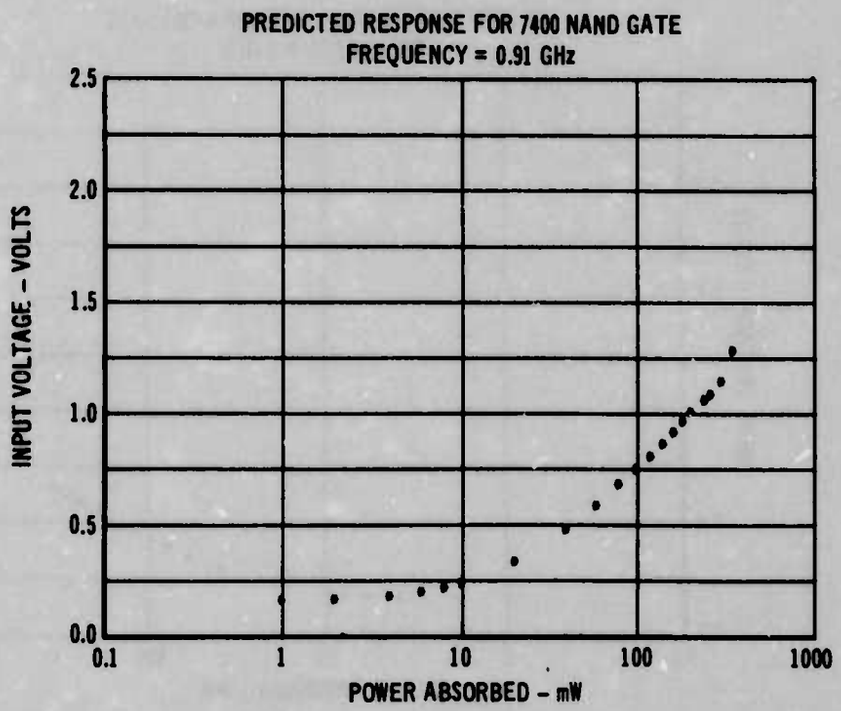


FIGURE 41 COMPARISON OF PREDICTED AND ACTUAL INTERFERENCE DATA FOR RF ENTERING THE INPUT, INPUT LOW BIAS STATE (0.91 GHz)

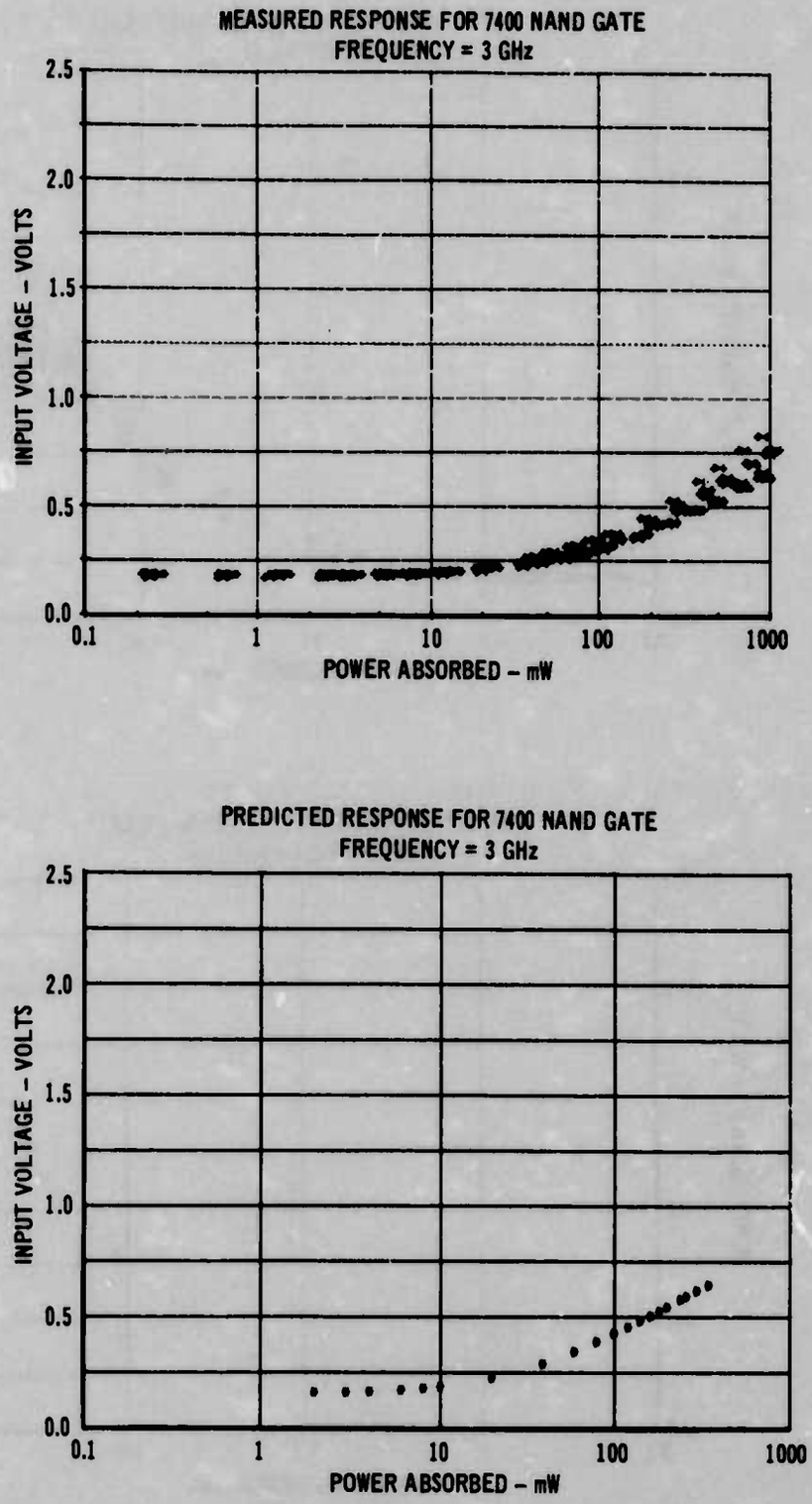


FIGURE 42 COMPARISON OF PREDICTED AND ACTUAL INTERFERENCE DATA FOR RF ENTERING THE INPUT, INPUT LOW BIAS STATE (3.0 GHz)

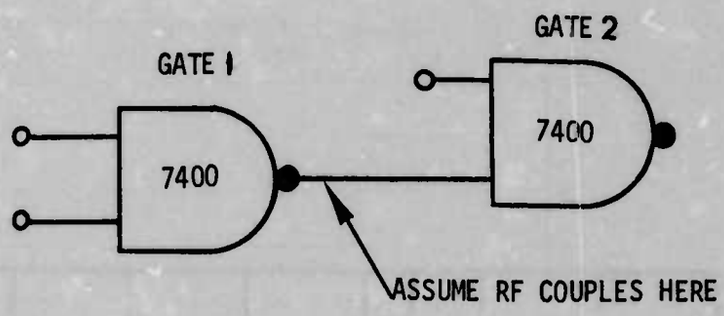


FIGURE 43 CIRCUIT DIAGRAM SHOWING TYPICAL INTERCONNECTION OF DEVICES FOR HYPOTHETICAL PROBLEM

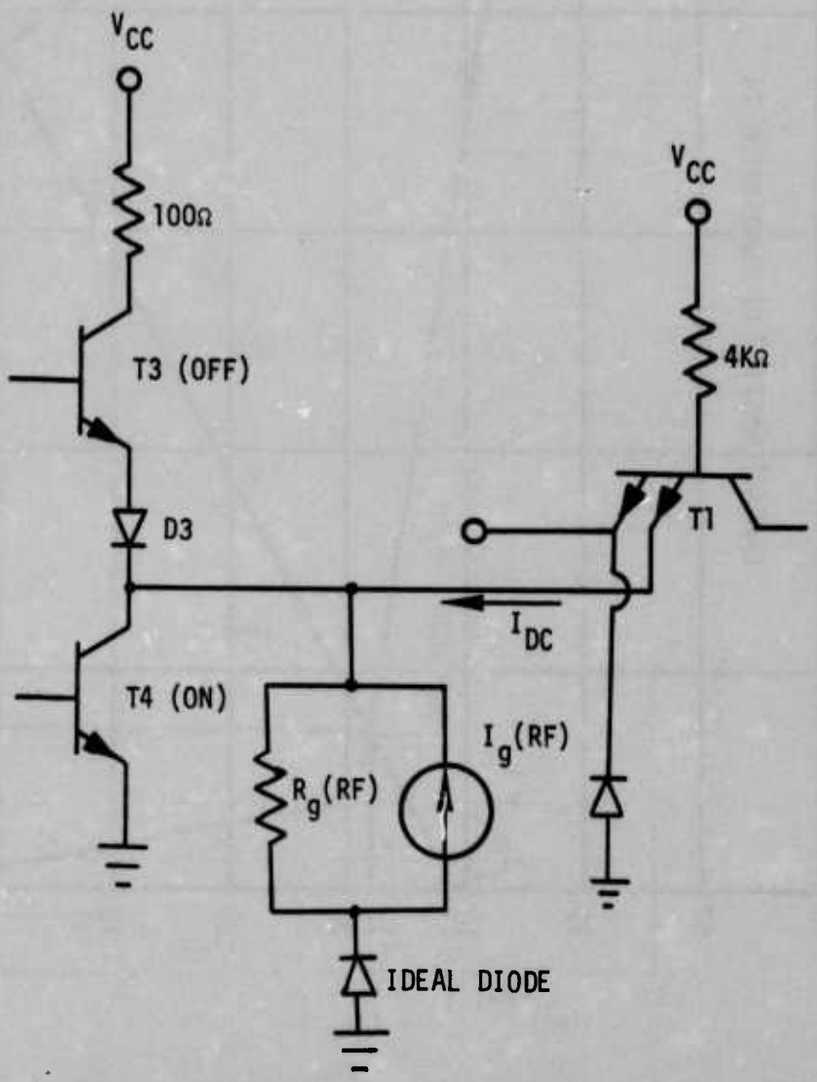


FIGURE 44 SCHEMATIC DIAGRAM SHOWING THE INTERNAL CIRCUITRY INVOLVED IN THE HYPOTHETICAL PROBLEM

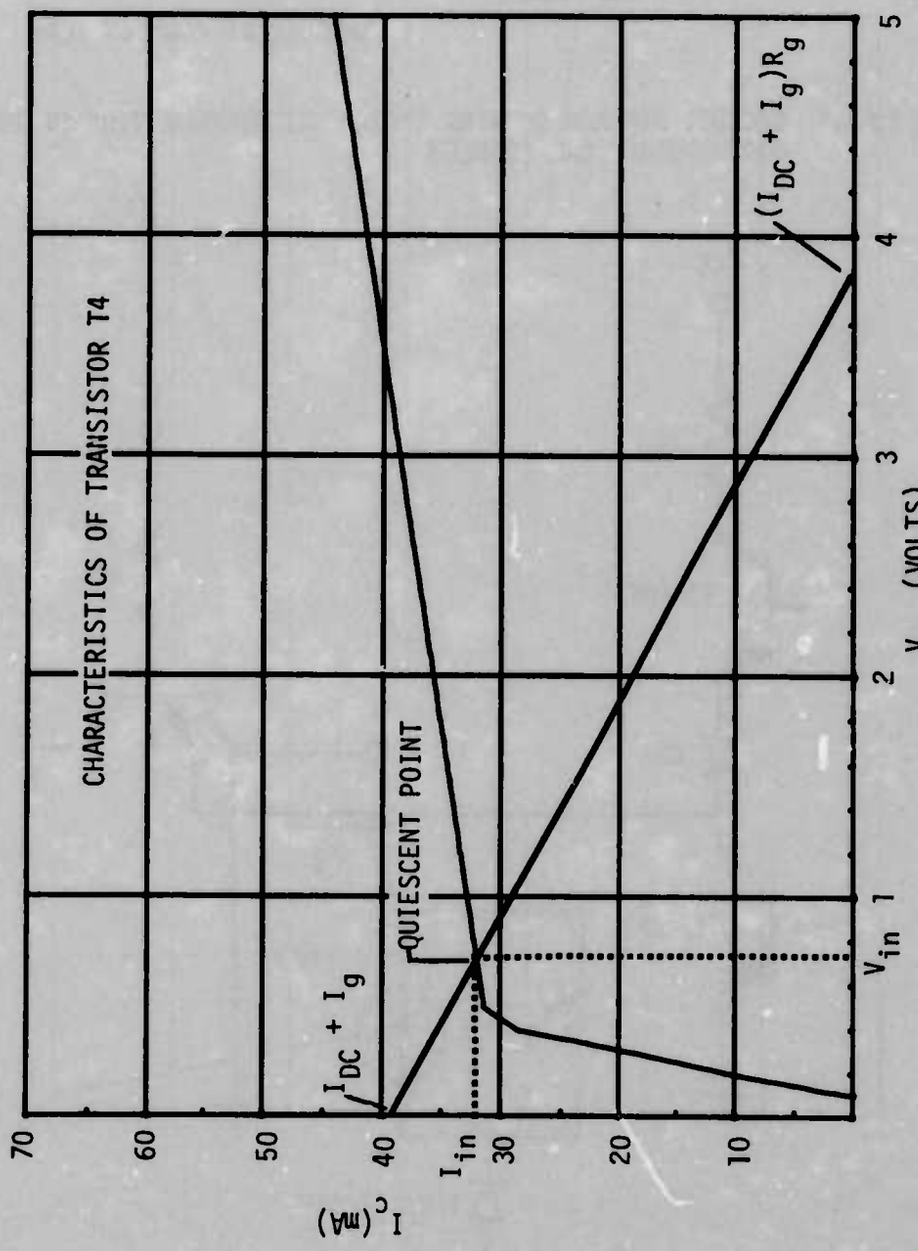


FIGURE 45 SOLUTION TO THE HYPOTHETICAL PROBLEM

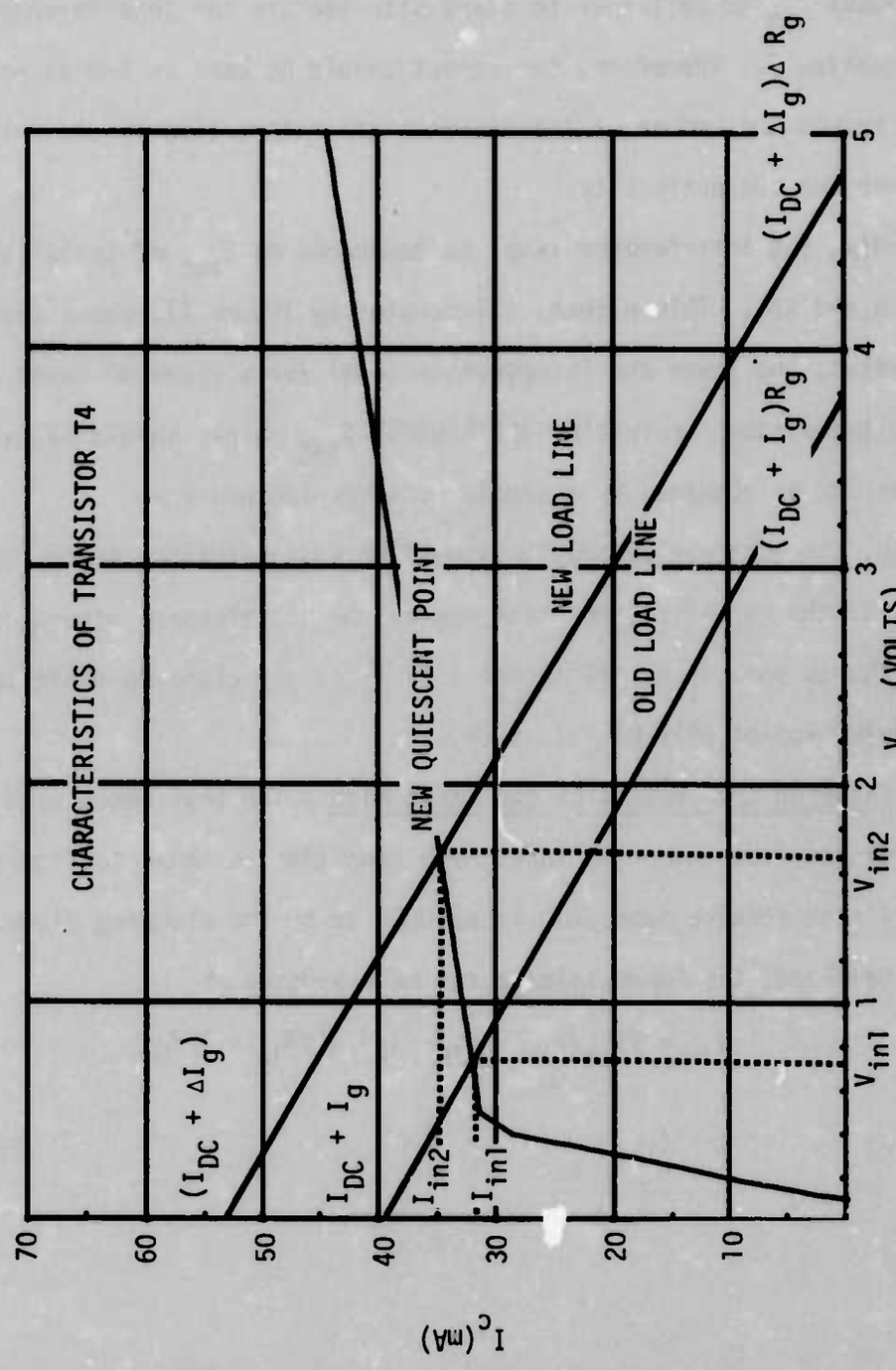


FIGURE 46 SOLUTION TO THE HYPOTHETICAL PROBLEM SHOWING THE EFFECT THAT INCREASING RF POWER HAS ON THE LOAD LINE

From this example, a few possibilities for reducing susceptibility appear. First of all, I_{DC}, which is a function of the number of inputs tied to the output of gate 1, causes V_{in} to be larger to start with (before the interference begins) as seen in equation 7. Therefore, the fanout should be kept as low as possible. This will also reduce the number of interference generators tied to the output and, hence, lower the susceptibility.

Secondly, the interference level is dependent on I_{sat} of transistor T4, (figures 45 and 46). This effect, illustrated by figure 47, shows that the higher the I_{sat} value, the lower the interference level for a given RF power. Therefore, gates with transistors exhibiting the highest I_{sat} values should be used. This information can be obtained by a simple DC screening process.

Lastly, the most obvious way to lower the susceptibility is to reduce the efficiency of the rectification which powers the interference generator. This can be done although some trade-off in the ability of the clamping diode to eliminate negative-going spikes will be sacrificed.

4.2.2 RF Entering the Input With the Input High - The test setup used to collect the interference data under the input high condition is shown in figure 48. Again the primary interference generator is assumed to be the clamping diode. With the generator in place, the input voltage can be expressed as

$$V_{in} = (V_{cc}/R_{in} - I_{DC} - I_g)/(1/R_{in} - 1/R_g) \qquad (8)$$

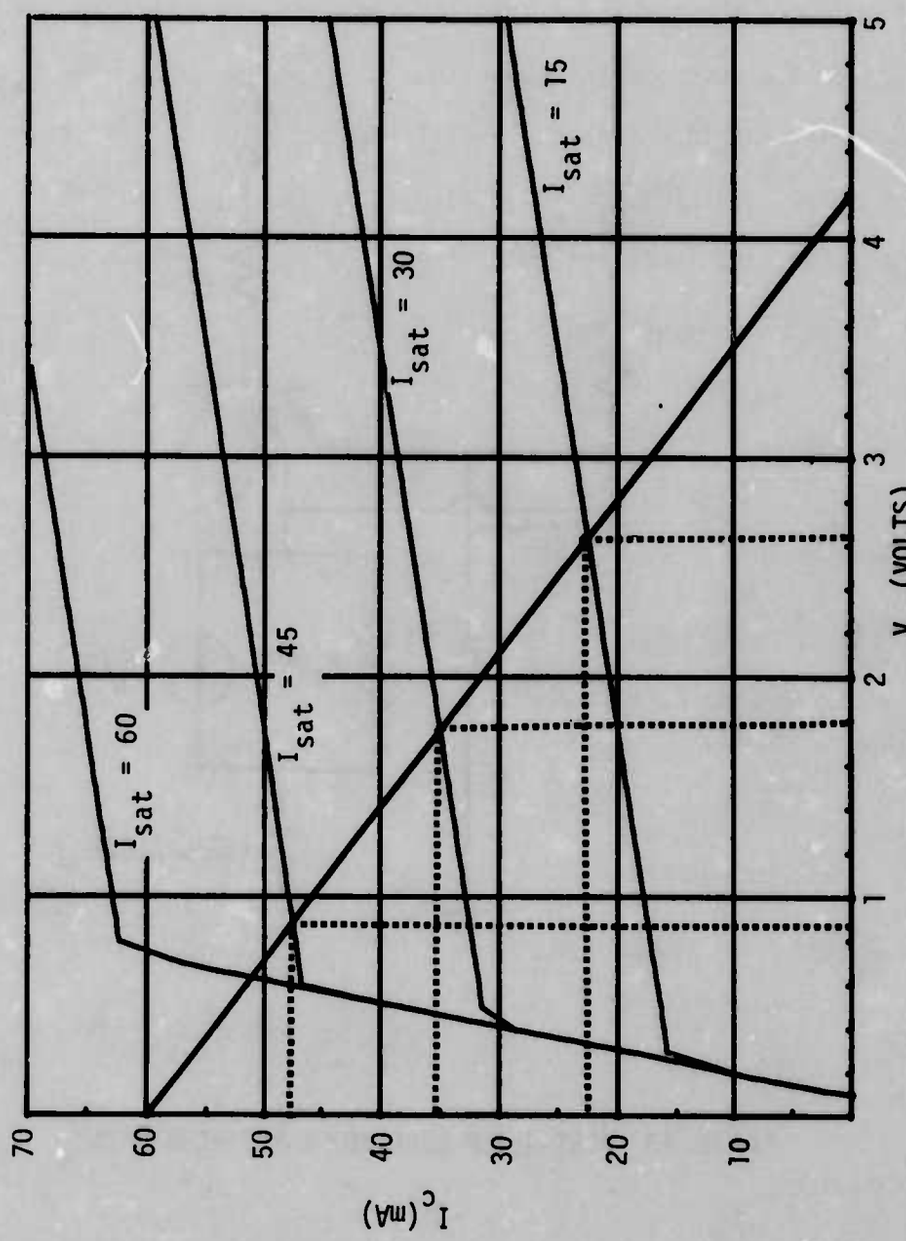


FIGURE 47 SOLUTION OF THE HYPOTHETICAL PROBLEM SHOWING THE EFFECT OF I_{sat} UPON THE QUIESCENT OPERATING POINT

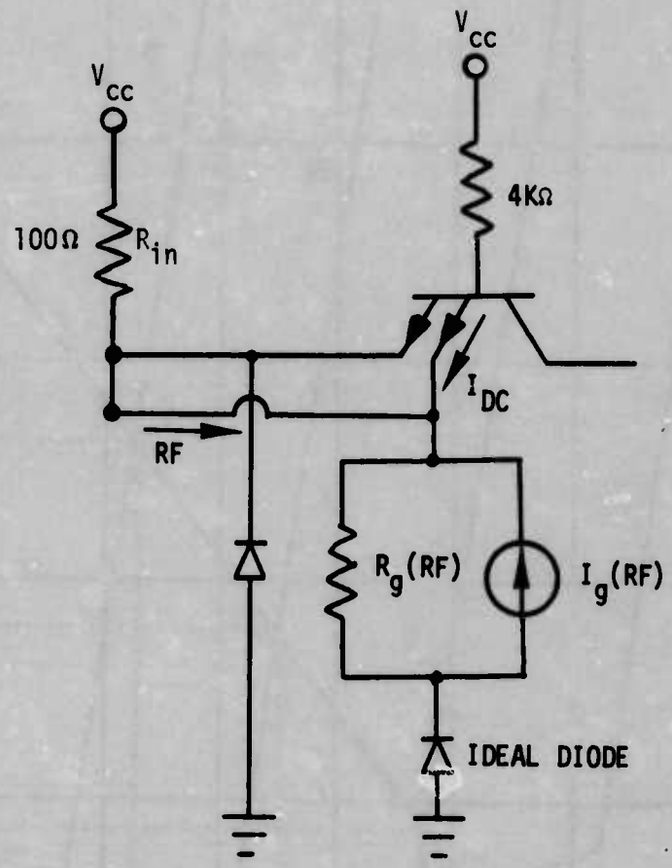


FIGURE 48 TEST SETUP USED FOR INPUT HIGH CASE

However, because the ideal diode is in series with the Norton generator, this equation is only valid when the product of I_g and R_g exceeds V_{cc}. Referring to the characteristics of the generator shown in figures 37 and 38, we see that this condition is never met. Therefore, equation 8 reduces to

$$V_{in} = V_{cc} - I_{DC}/R_{in} \quad (9)$$

Typically, I_{DC} is very small because the base emitter junction of T1 is reversed biased and hence V_{in} is approximately equal to V_{cc}. Our prediction then, based upon the Norton generator, is that no interference will be observed. But, by examination of the interference data collected (and shown in figure 49), we see that another effect becomes operative. Evidently, transistor T1 is somehow causing the observed effect of current flowing into the device, possibly by inverse transistor operation. The transistor is biased for inverse operation, but the reverse characteristics are so poor (by deliberate design) that this phenomenon does not occur normally. Evidently, the RF signal is rectified in the base-collector region

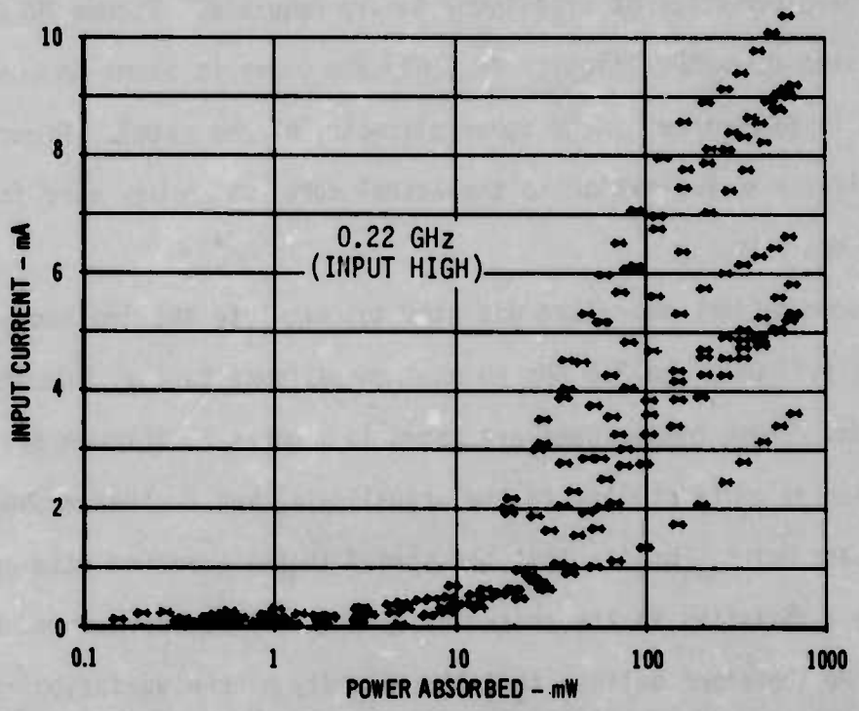


FIGURE 49 INPUT CURRENT VS RF POWER FOR RF ENTERING THE INPUT, INPUT HIGH - OUTPUT LOW BIAS STATE

and provides a bias current which is greatly amplified to produce the observed results. This phenomenon is important for the case of RF entering a high input when the other is low. A quick look experiment verified that the device was susceptible in this mode, but no detailed measurements were made. This phenomenon needs further exploration as it should be quite significant in other device types.

4.2.3 RF Entering the Output With Output Low - As was stated earlier, the parasitic diode which shunts transistor T4 is believed to be the primary cause for the interference observed at the output. The characteristics of the interference generator representing this diode are shown in figures 50 and 51. Referring to figure 52, the output voltage can be written as

$$V_{out} = V_{ce} = (I_f(max) + I_g - I_c)\left(\frac{V_{cc}}{I_f(max) + \frac{V_{cc}}{R_g}}\right) \qquad (10)$$

where I_f = fanout (sink) current.

In order to solve equation 10 and make comparisons with the interference data, the collector characteristics of transistor T4 are required. Figure 53 shows an example of the measured characteristics of T4 (only one curve is shown because the base drive to T4 is determined by the other circuitry of the gate). Figure 54 shows a piece-wise linear approximation to the actual curve which was used for this preliminary analysis.

The procedure just described was used to calculate the implied output voltage at 0.22 GHz, 0.91 GHz, and 3.0 GHz so that comparisons to the interference data could be made. These comparisons are shown in figures 55 through 57. The form of the prediction is quite similar to the actual data, but further refinement is needed to get an exact match. Notice that the spread in the observed data appears to be explained by a variation in the characteristics of T4 as represented by the I_{sat} parameter. We therefore believe that the majority of the variation observed in this interference data is due to the difference in characteristics of transistor T4 over the sample.

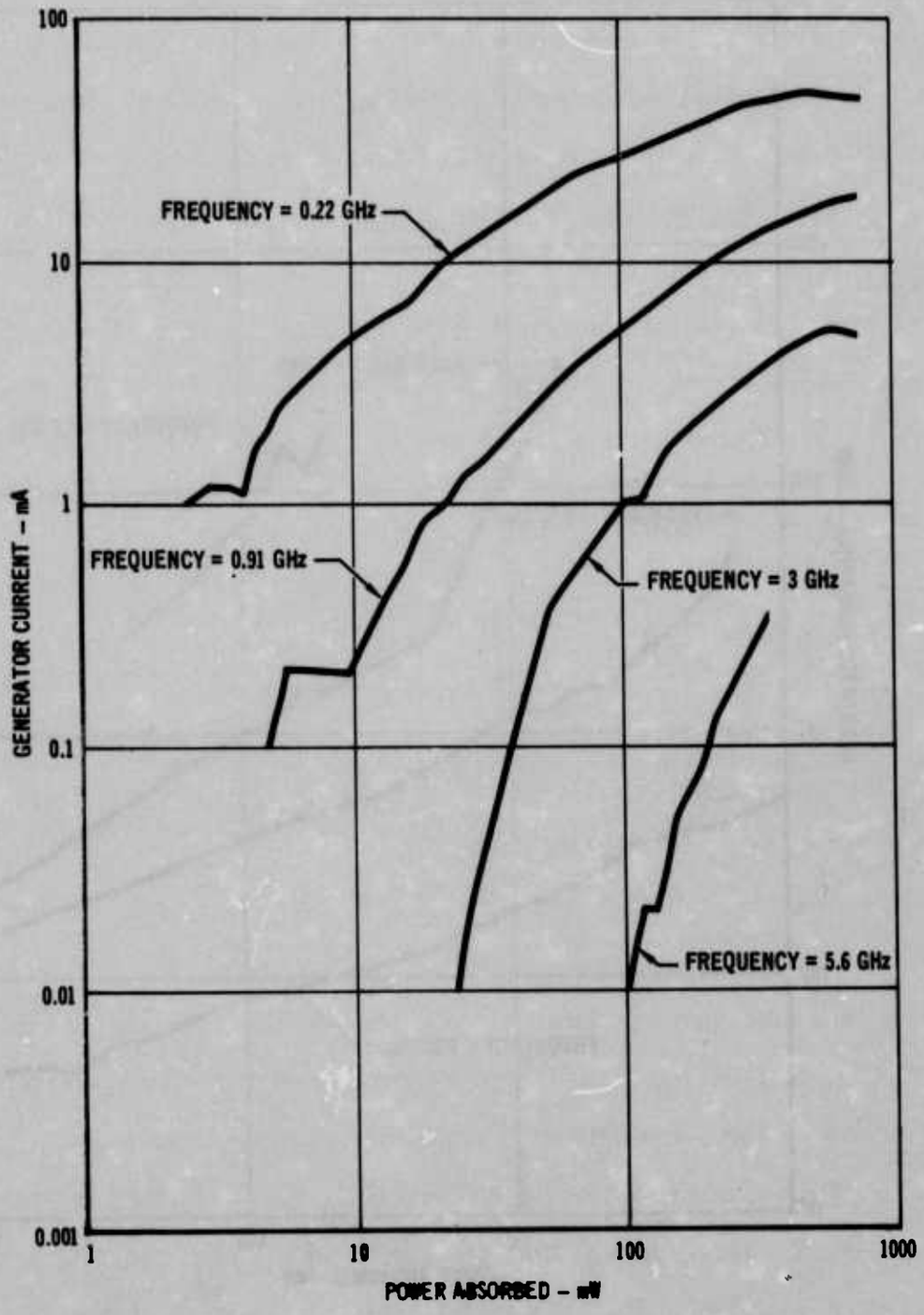


FIGURE 50 CHARACTERISTICS OF I_g FOR THE OUTPUT PARASITIC DIODE

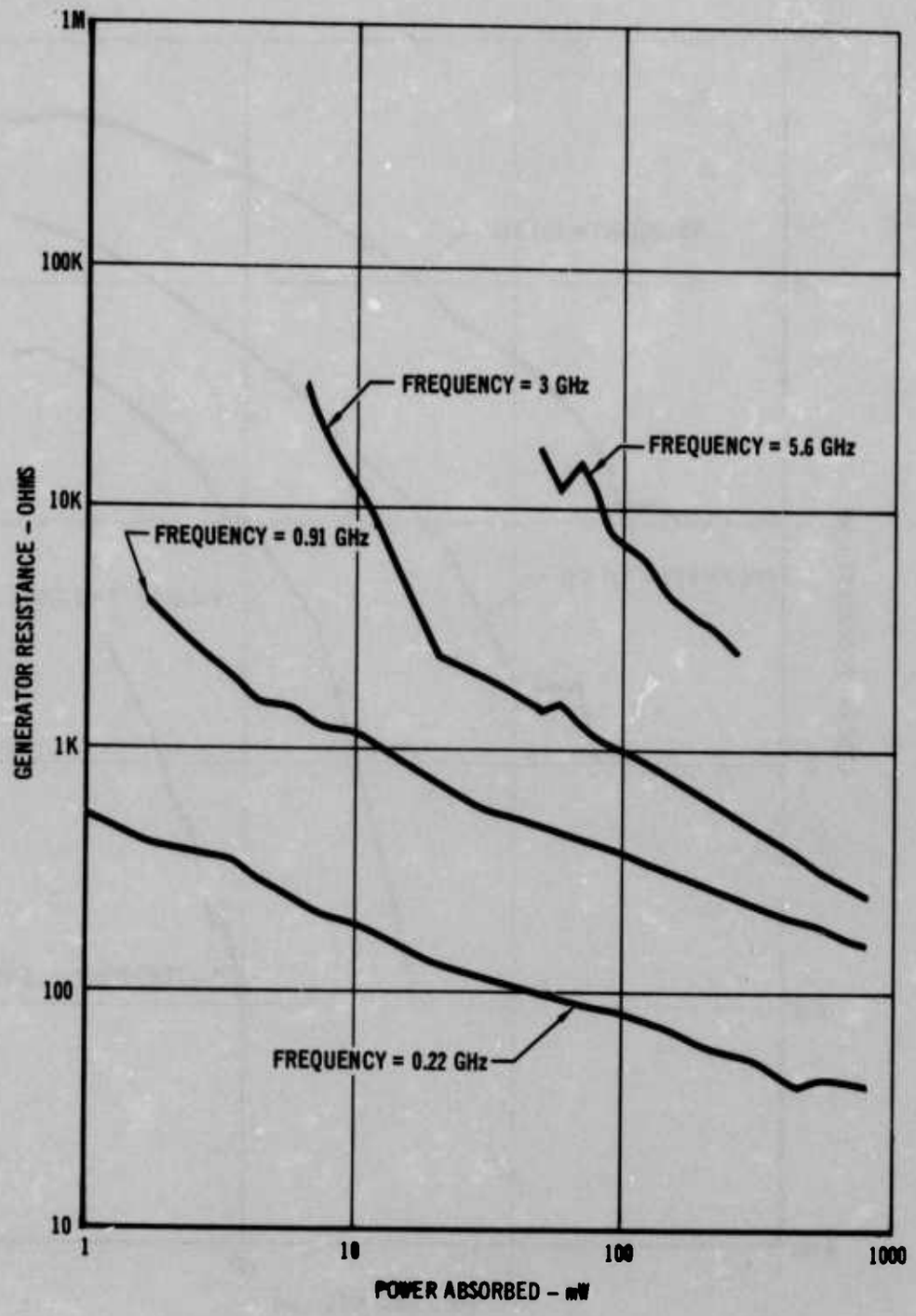


FIGURE 51 CHARACTERISTICS OF R_g FOR THE OUTPUT PARASITIC DIODE

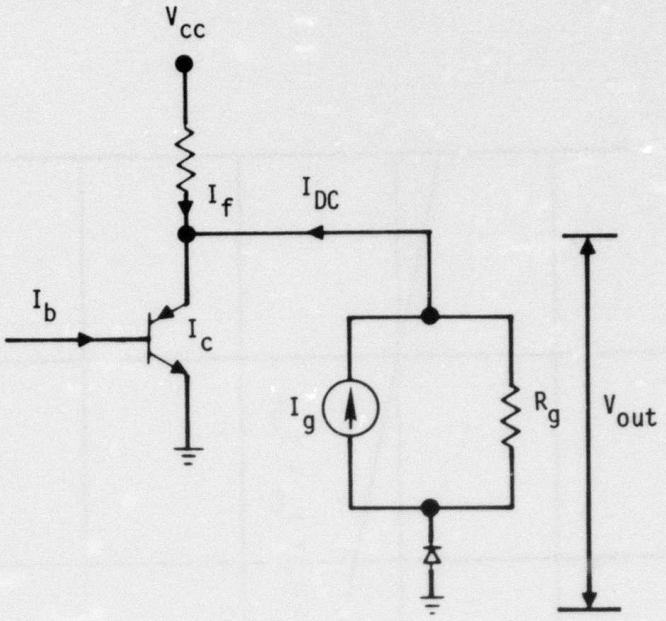


FIGURE 52 EQUIVALENT CIRCUIT OF THE OUTPUT OF THE 7400 (OUTPUT LOW CASE)

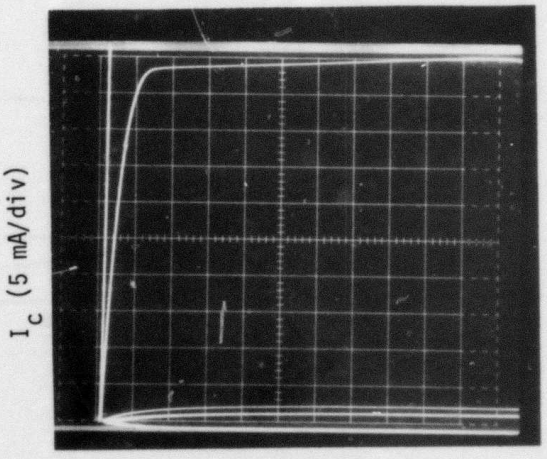


FIGURE 53 PHOTOGRAPH OF COLLECTOR CHARACTERISTIC OF T4

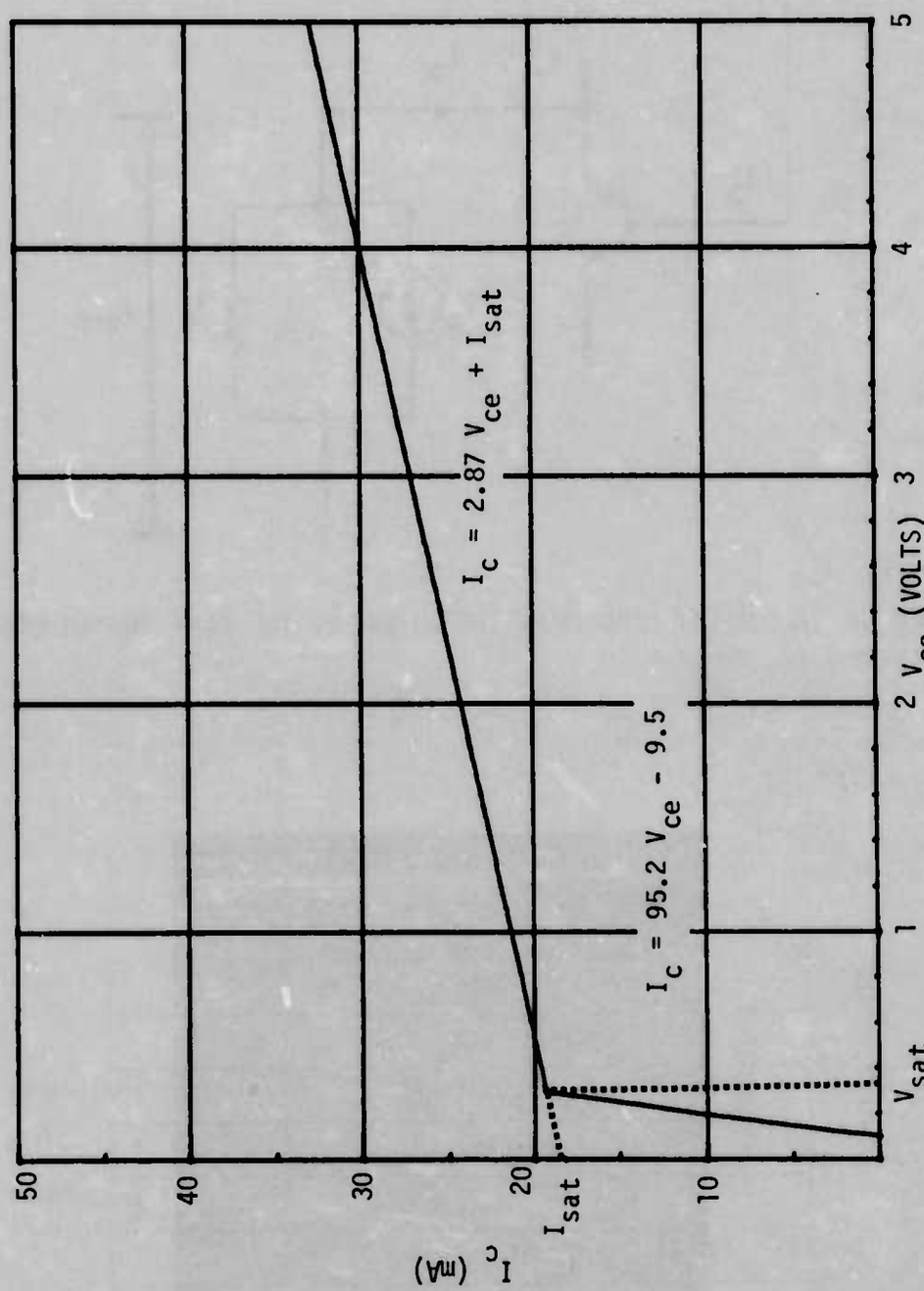
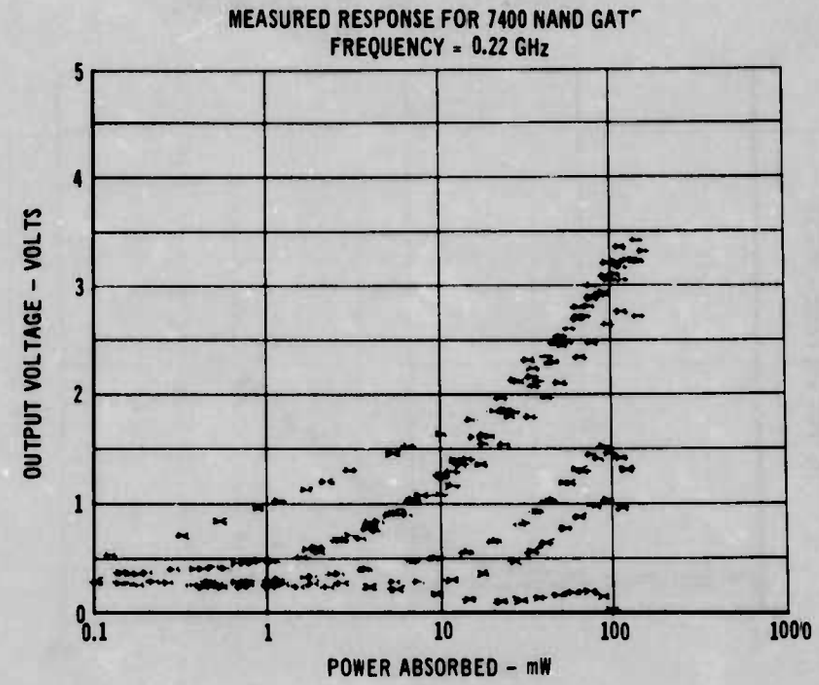


FIGURE 54 PIECEWISE LINEAR APPROXIMATION OF T4 CHARACTERISTICS



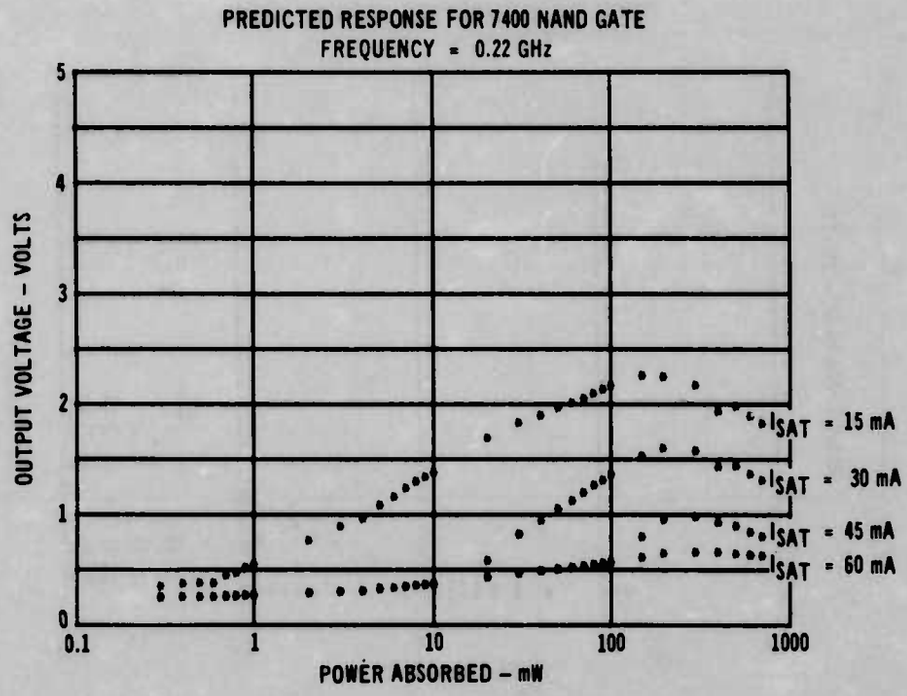


FIGURE 55 COMPARISON OF PREDICTED AND ACTUAL INTERFERENCE DATA FOR RF ENTERING THE OUTPUT, OUTPUT LOW BIAS STATE (0.22 GHz)

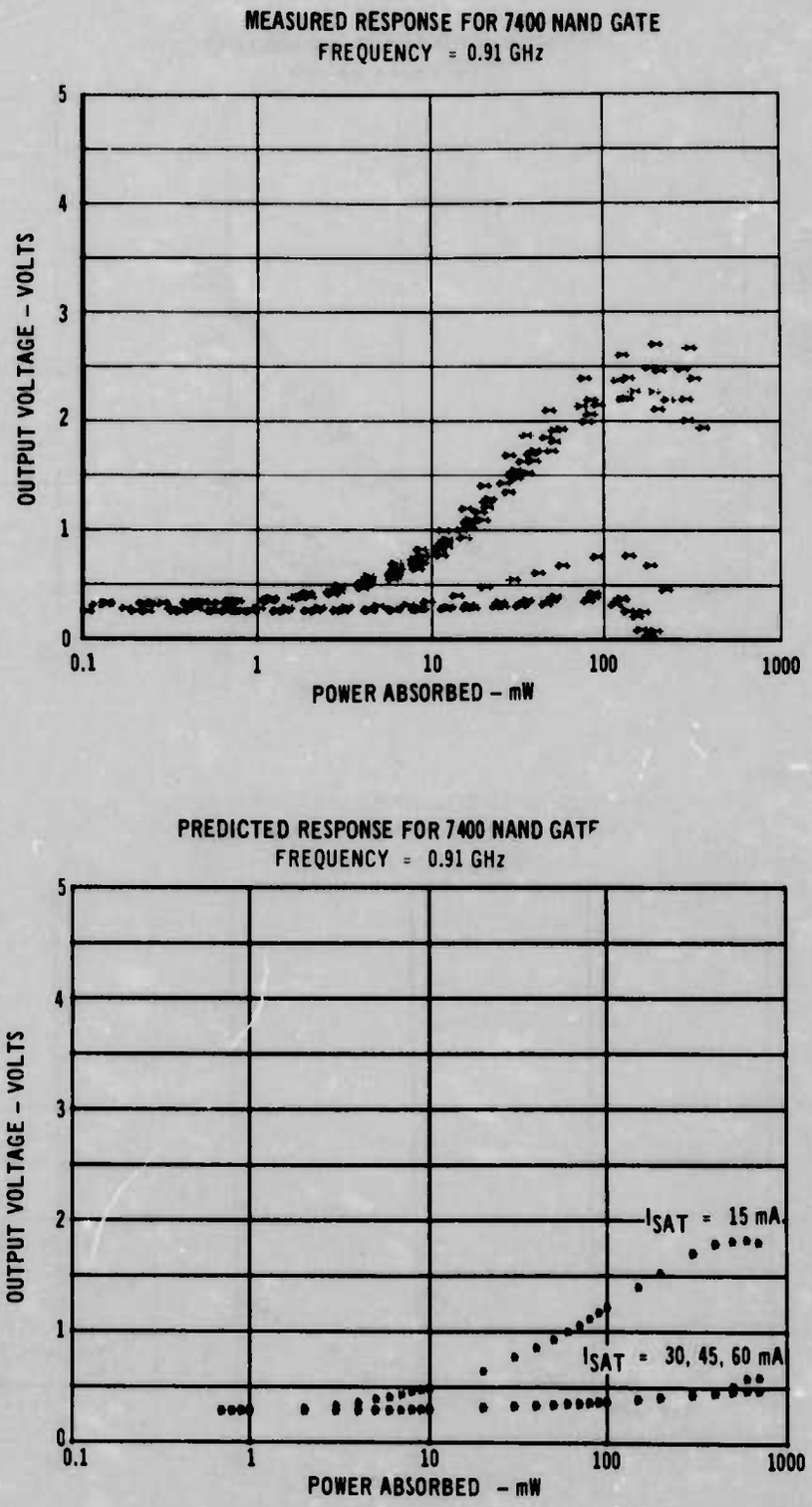
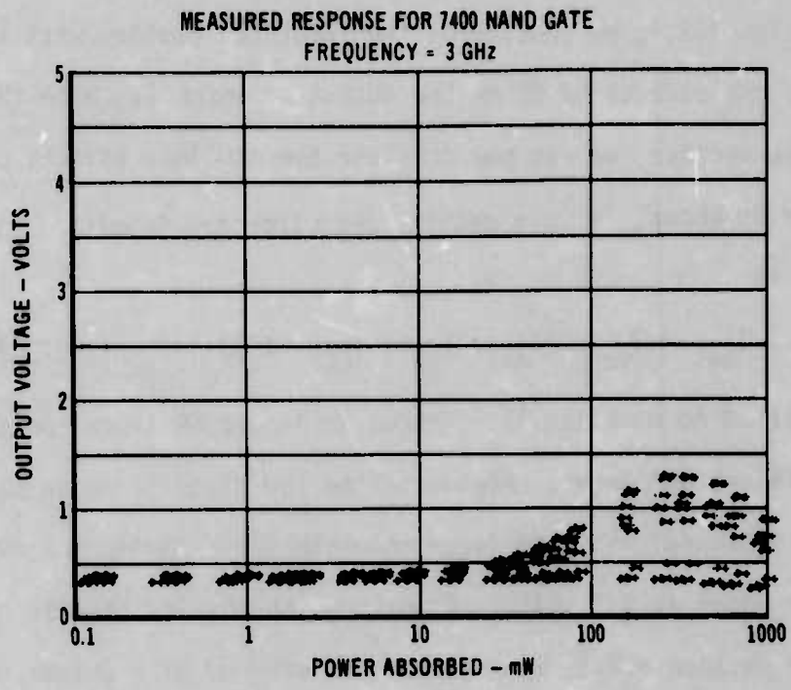


FIGURE 56 COMPARISON OF PREDICTED AND ACTUAL INTERFERENCE DATA FOR RF ENTERING THE OUTPUT, OUTPUT LOW BIAS STATE (0.91 GHz)



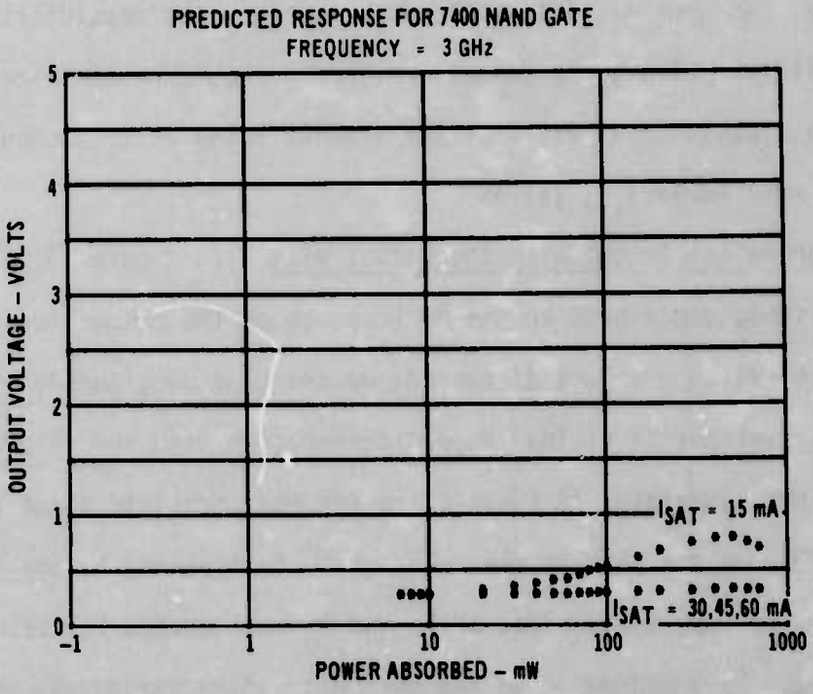


FIGURE 57 COMPARISON OF PREDICTED AND ACTUAL INTERFERENCE DATA FOR RF ENTERING THE OUTPUT, OUTPUT LOW BIAS STATE (3.0 GHz)

To extend our predictions, consider the problem outlined in figure 58. As treated in section 4.2.1, we considered the identical problem with the exception that we ignored the effects of RF on the output of gate 1. With the information obtained in this section, we can now consider the combined effects of the input and output. Figure 59 shows, in more detail, the circuitry involved. The equation for output voltage is

$$V_{out} = V_{ce} = (I_{g1} + I_{g2} + I_{DC} - I_c)/(1/R_{g1} + 1/R_{g2}) \qquad (11)$$

A supposed solution to equation 11 is shown in figure 60 since the exact characteristics of transistor T4 are not known. Again, if the low state is to be maintained, the load line must intersect the transistor characteristic curve at a point such that V_{ce} is less than or equal to 0.8 volts. Comparing the results of this problem to that hypothesized in section 4.2.1, we see that the chances of a change in state occurring are even greater.

As before, two general statements can be made on the possibilities of reducing the susceptibility. First, the fanout or loading should be minimized, and second, gates in which transistor T4 exhibits the highest value of I_{sat} should be used in lieu of those with lower I_{sat} values.

4.2.4 RF Entering the Output With the Output High - In figure 31, all the generators that could possibly contribute to the RF response of the output were shown. In the output-low case, which was just discussed, we saw that considering only the diode which shunts transistor T4 yielded a good correlation with the interference data. However, when this generator is substituted for the parasitic diode in the output-high case (figure 33), we see that it can not contribute anything to the response. The reason for this is that the product of I_g and R_g must exceed V_{cc} before its effects will be noticed. By examination of the generator characteristics, we see that these conditions were never met.

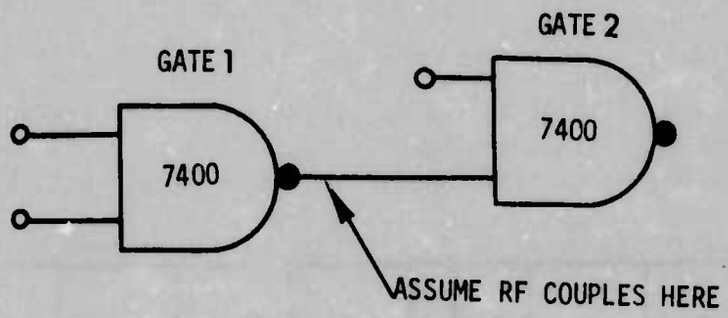


FIGURE 58 HYPOTHETICAL PROBLEM

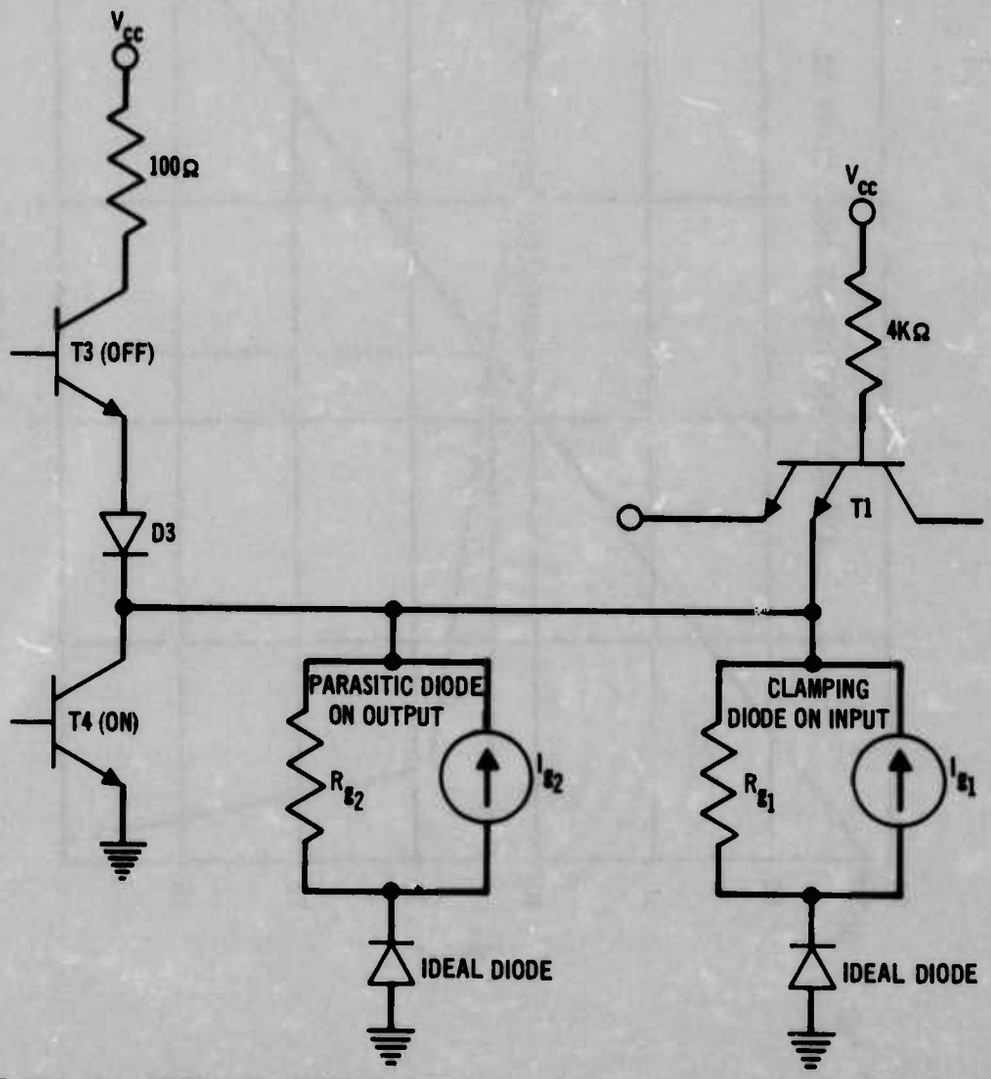


FIGURE 59 DETAILED DRAWING SHOWING INTERFERENCE GENERATORS PRESENT IN BOTH GATES

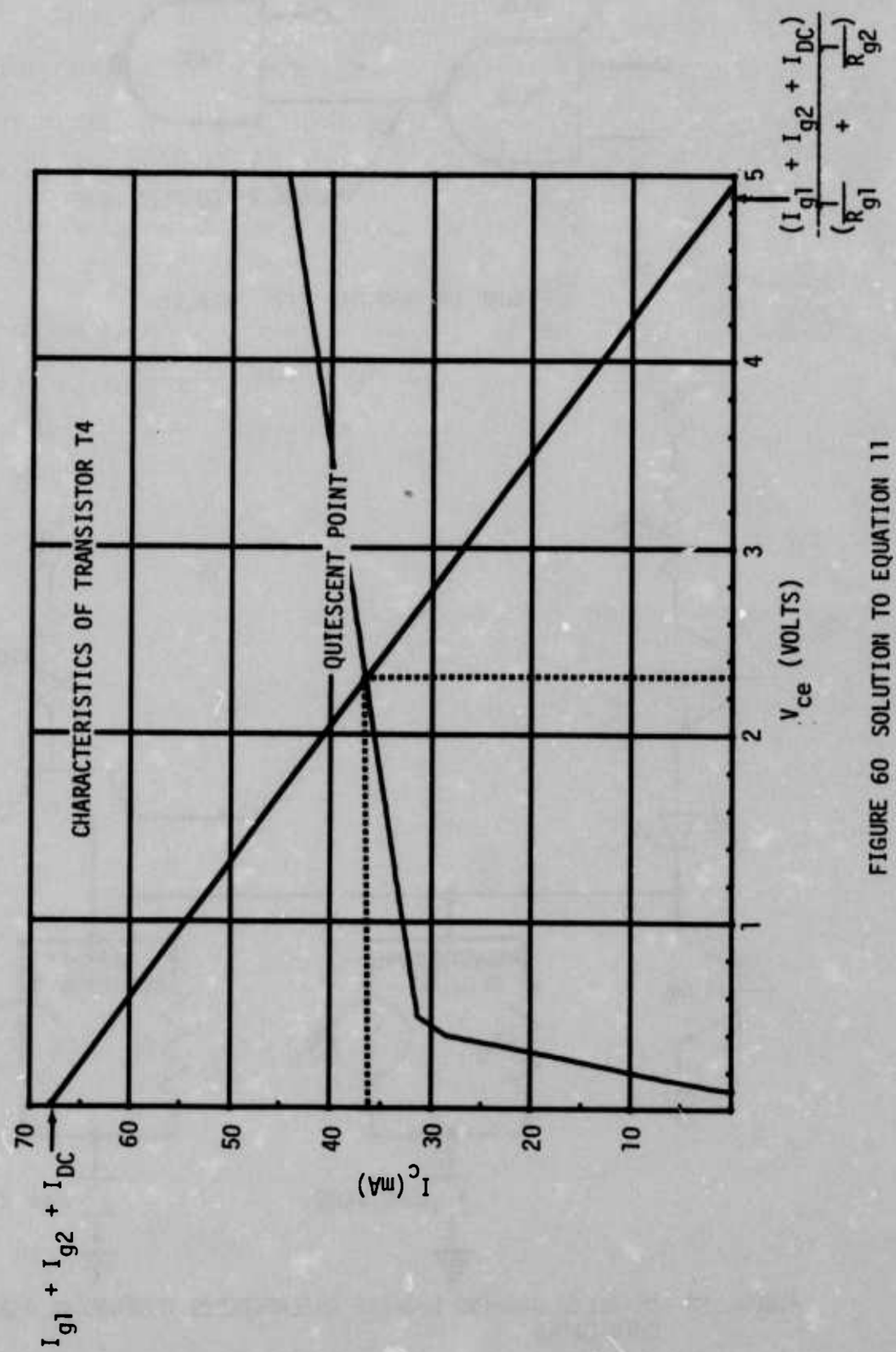


FIGURE 60 SOLUTION TO EQUATION 11

A closer look at the possible interference generators leads one to believe that somehow D3 is contributing to the response as shown in figure 61. The interference data taken under these conditions, shown in figure 62, indicates that it is possible for a generator in this position to contribute in a manner to support the observed interference. Because the data necessary to define the interference generator for D3 are not available, we are presently unable to make a comparison with the interference measurements.

Even though the comparisons cannot be made, this case seems to be, at present, of little importance as far as susceptibility is concerned. The reason being that no change in state is likely to occur.

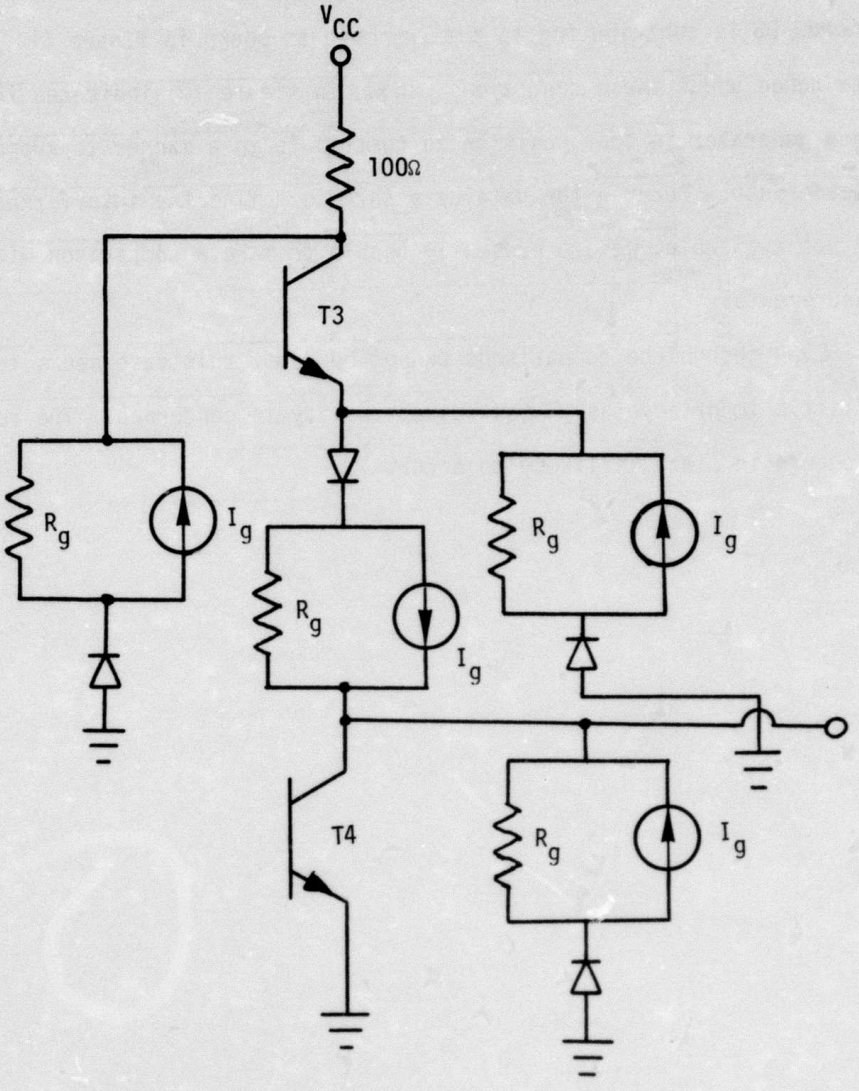


FIGURE 61 POSSIBLE RECTIFICATION SITES APPEARING AT THE OUTPUT

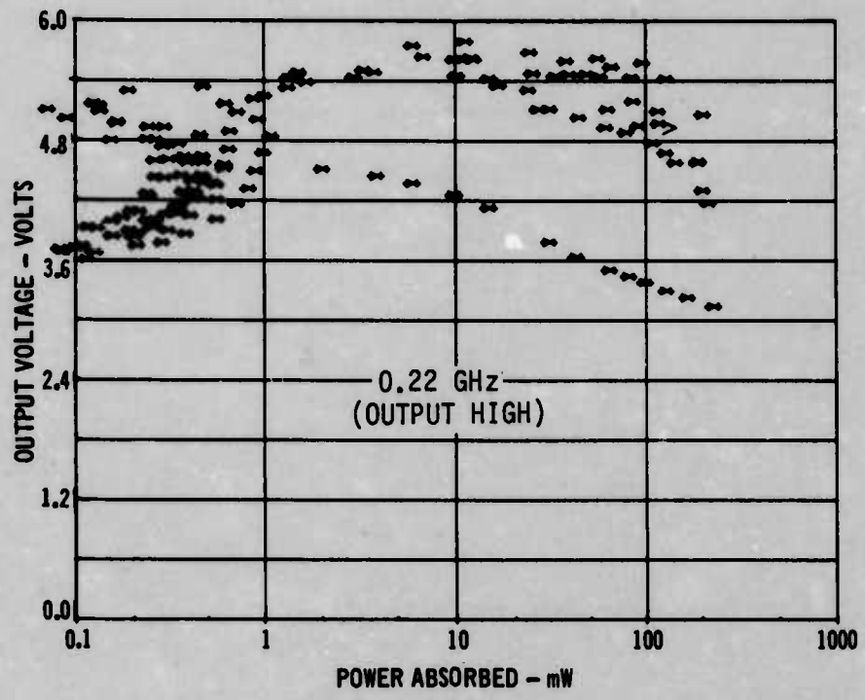


FIGURE 62 PLOT OF THE OUTPUT VOLTAGE VERSUS RF POWER FOR RF ENTERING THE OUTPUT - OUTPUT HIGH BIAS STATE

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5. CONCLUSIONS

The 7400 NAND gate, as a representative of the broad class of bipolar digital devices, has been thoroughly examined to determine what happens when microwave energy is injected into its various ports. Numerous effects have been observed and documented; some of which can be considered quite significant to system designers who must build electronic systems that will operate in severe electromagnetic environments. In particular, certain combinations of injection port and device operating state exhibit complete change-of-state at relatively low absorbed power levels. At higher stimulus levels, catastrophic failure (burnout) is observed.

Analysis of the data has shown that rectification in the various pn junctions of the device will explain most of the interference effects observed. The rectification sites can be modelled as interference sources using Norton or Thevenin equivalent circuits with empirically-determined parameters. The manifestation of the interference sources on the device output or input signals depends upon both external load conditions and internal device parameters. It is possible to model the first order effects in a satisfactory manner, but a firm understanding of higher order effects will require further analysis. In particular, work is recommended to determine the RF coupling factors across the chip to internal junctions, to investigate the inverse transistor action on the input, and to determine the limitations to generalization imposed by the external loading used to simulate normal operating conditions.

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REFERENCES

1. "Integrated Circuit Electromagnetic Susceptibility Investigation - Bipolar Op Amp Study", MDC Report E1124, dated 9 August 1974. Prepared under contract number N00178-73-C-0362 for the U. S. Naval Weapons Laboratory by McDonnell Douglas Astronautics Company - East, St. Louis, Missouri 63166.

2. "Integrated Circuit Electromagnetic Susceptibility Investigation - Development Phase Report", MDC Report E0690, dated 19 October 1974. Prepared under contract N00178-72-C-0213 for the U. S. Naval Weapons Laboratory by McDonnell Douglas Astronautics Company - East, St. Louis, Missouri 63166.

3. "Integrated Circuit Electromagnetic Susceptibility Investigation - Test and Measurement Systems", MDC Report E1099, dated 12 July 1974. Prepared under contract number N00178-73-C-0362 for the U. S. Naval Weapons Laboratory by McDonnell Douglas Astronautics Company - East, St. Louis, Missouri 63166.

4. Ginzton, Edward L., Microwave Measurements, McGraw-Hill Book Company, Inc. New York, 1957.

5. Sucher, et. al., Handbook of Microwave Measurements, Polytechnic Institute of Brooklyn, 55 Johnson Street, Brooklyn, New York, 1963.

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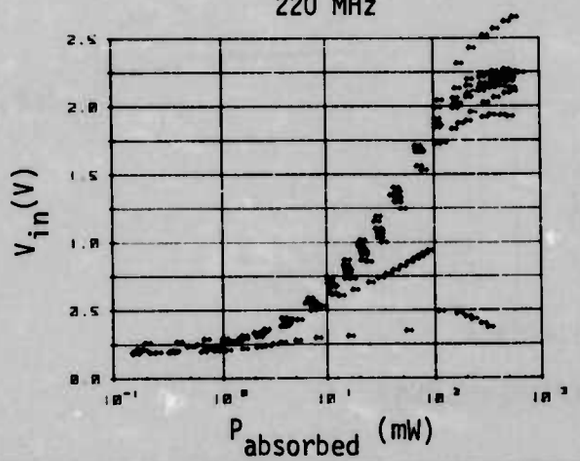
APPENDIX A

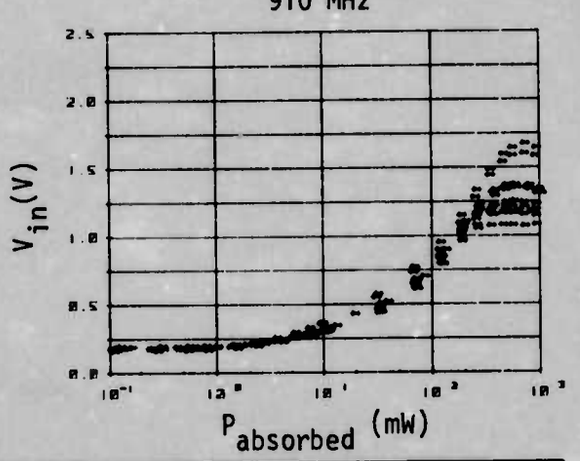
7400 INTERFERENCE DATA

7400 INTERFERENCE DATA

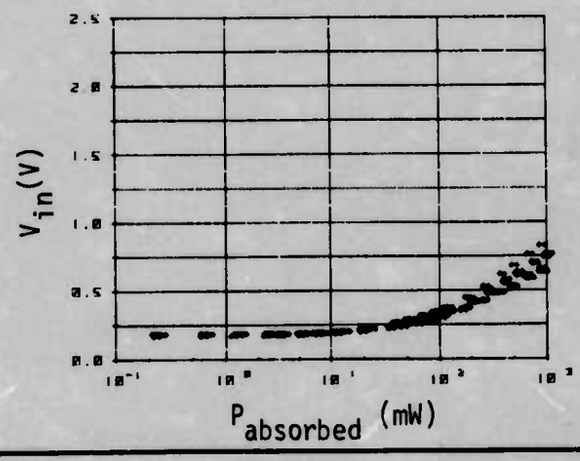
220 MHz



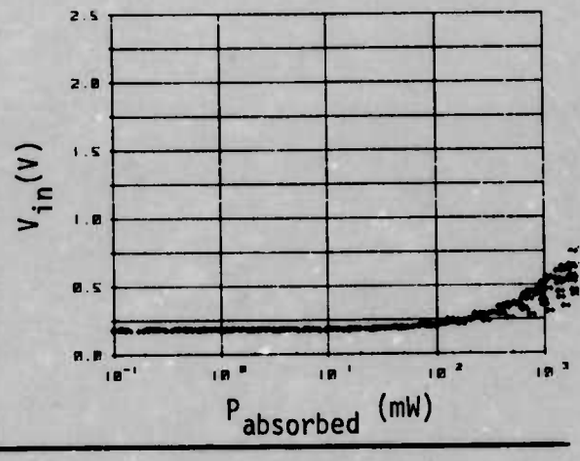
910 MHz



3.0 GHz

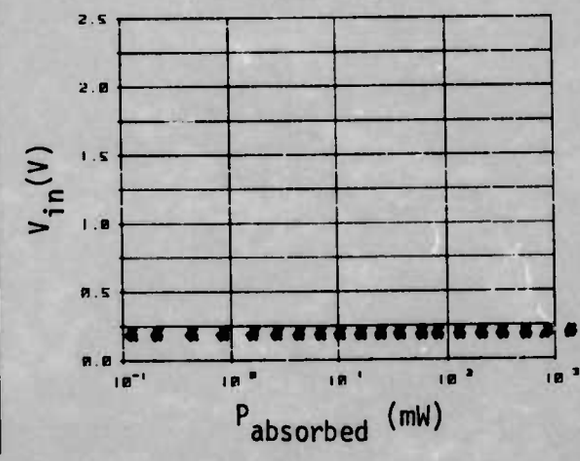


5.6 GHz



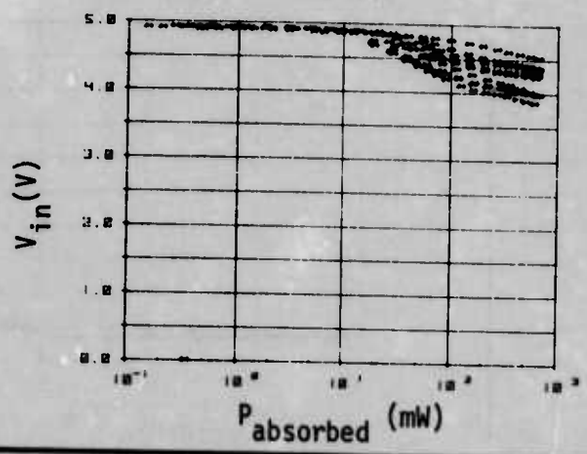
RF INJECTED INTO INPUT
INPUT LOW - OUTPUT HIGH

9.1 GHz



7400 INTERFERENCE DATA

220 MHz



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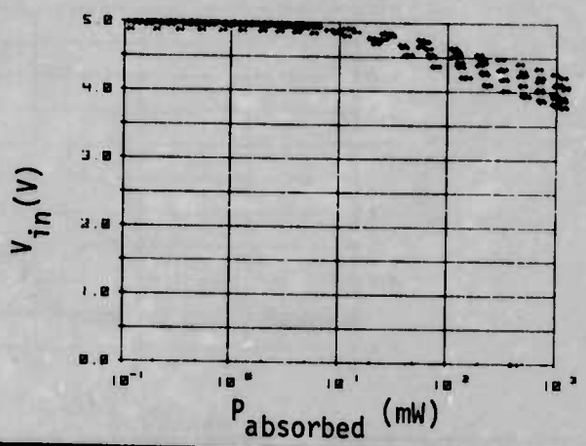
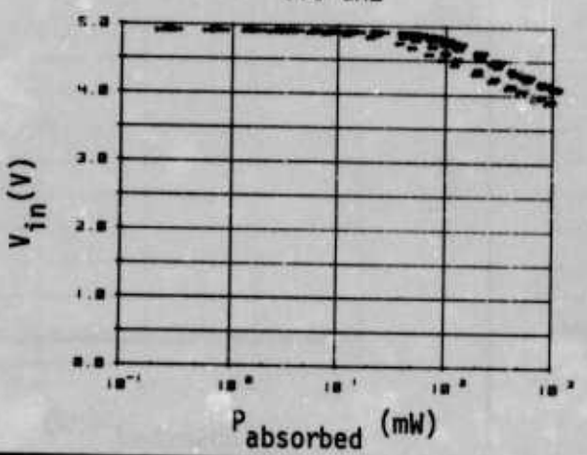
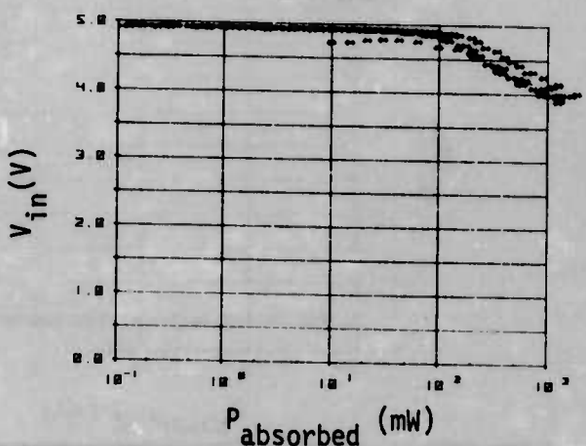


3.0 GHz



5.6 GHz



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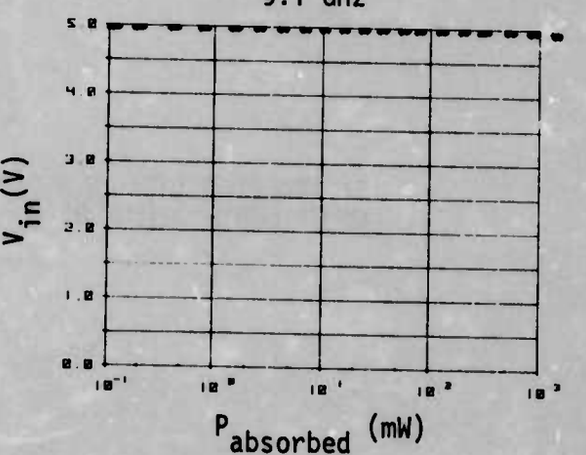
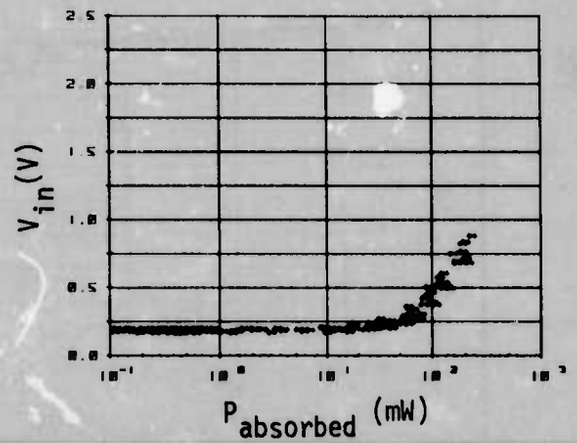


RF INJECTED INTO INPUT
INPUT HIGH - OUTPUT LOW

7400 INTERFERENCE DATA

220 MHz



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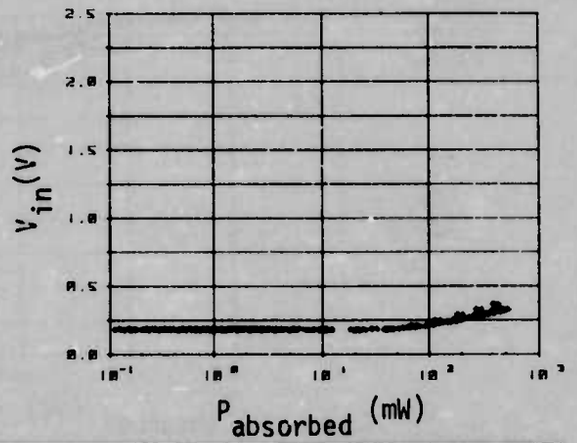
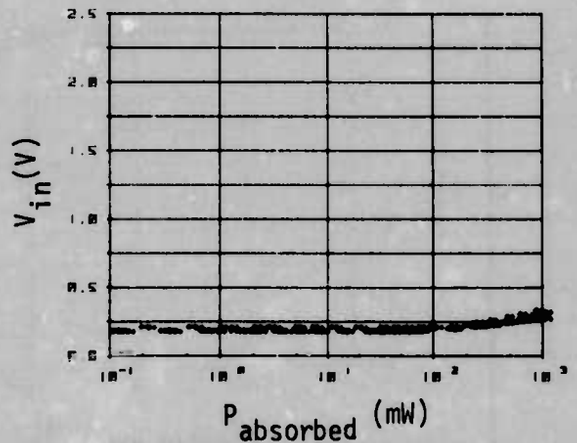
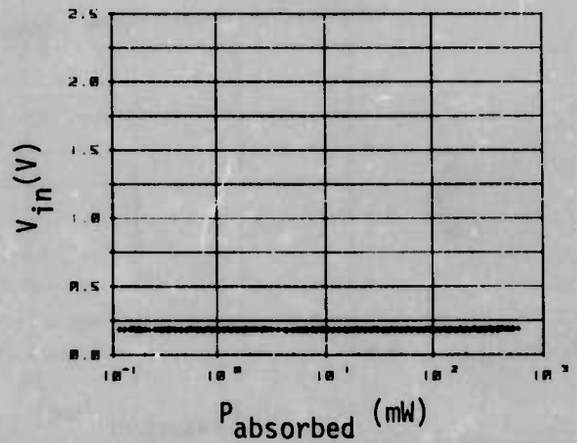


3.0 GHz

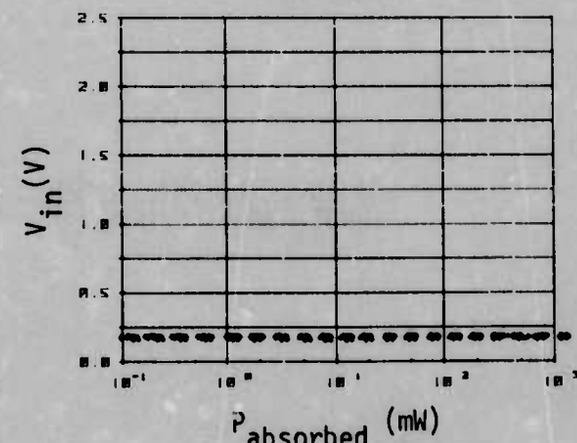


5.6 GHz



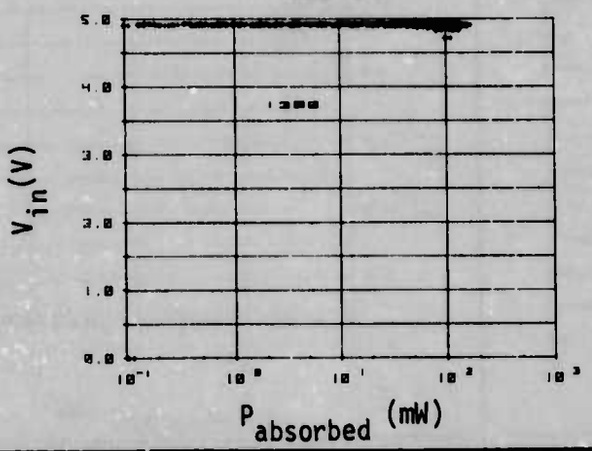
RF INJECTED INTO OUTPUT
INPUT LOW - OUTPUT HIGH

9.1 GHz

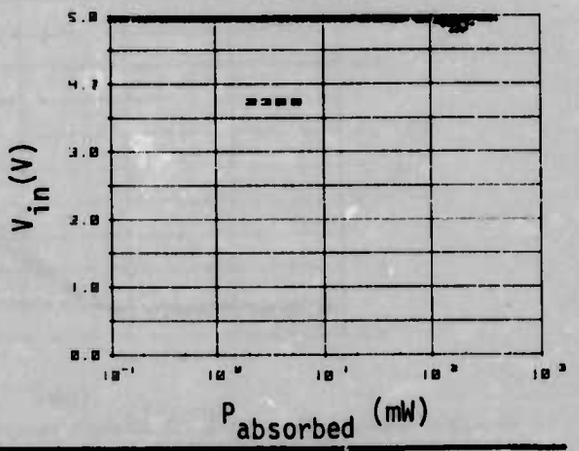


7400 INTERFERENCE DATA

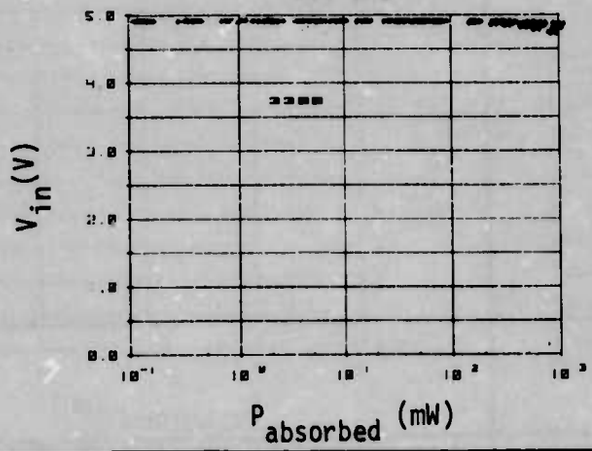
220 MHz



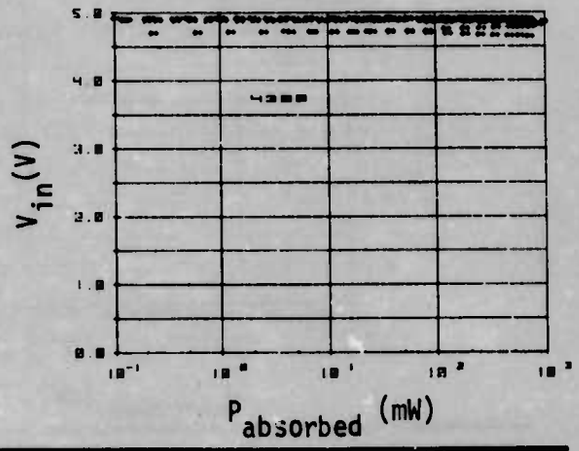
910 MHz



3.0 GHz

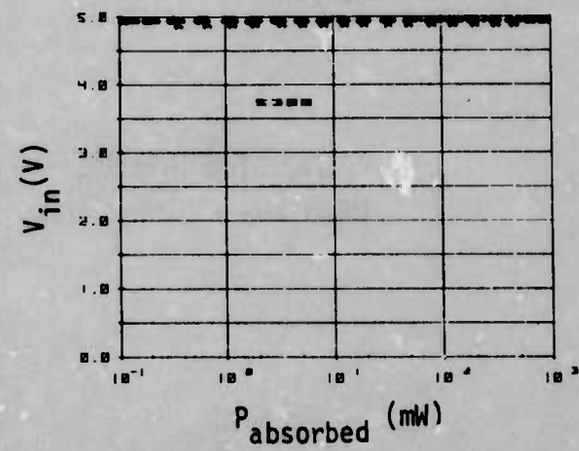


5.6 GHz



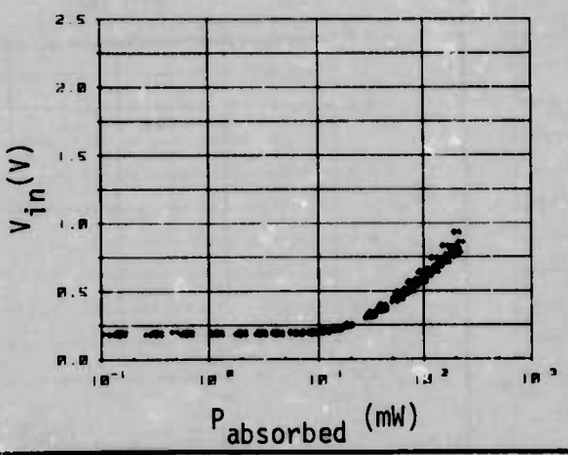
RF INJECTED INTO OUTPUT
INPUT HIGH - OUTPUT LOW

9.1 GHz

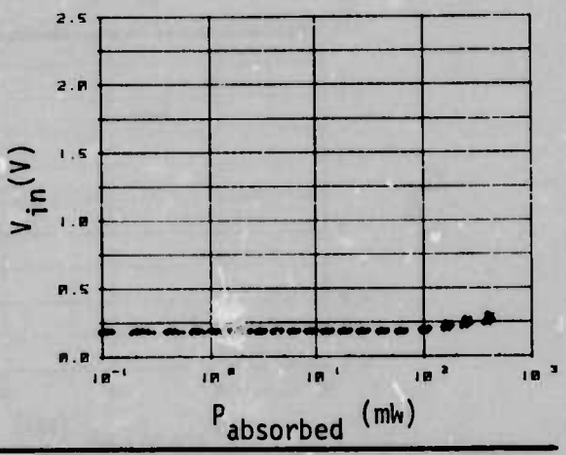


7400 INTERFERENCE DATA

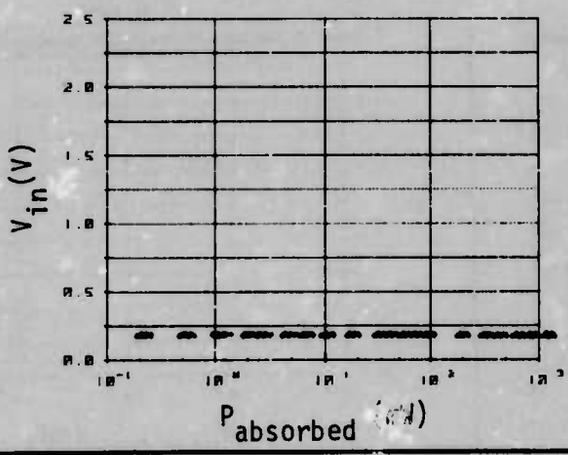
220 MHz



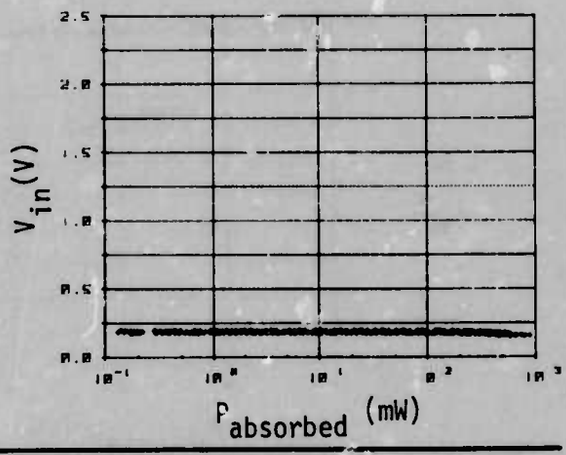
910 MHz



3.0 GHz

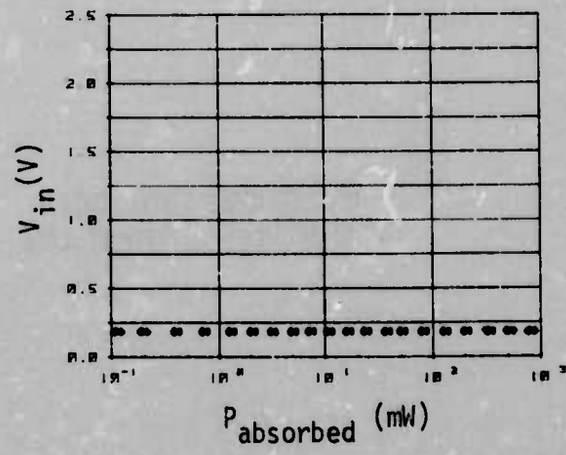


5.6 GHz



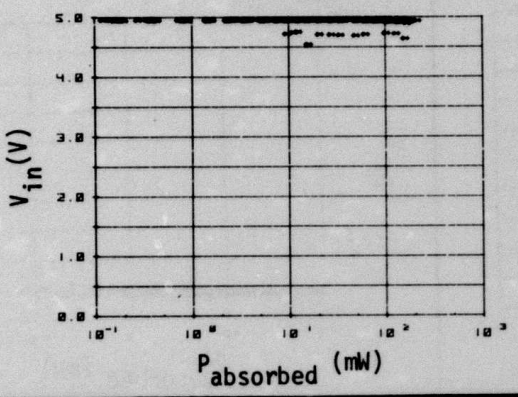
RF INJECTED INTO V_{CC}
INPUT LOW - OUTPUT HIGH

9.1 GHz

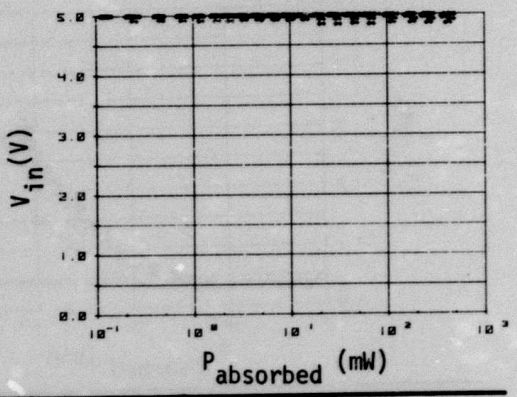


7400 INTERFERENCE DATA

220 MHz



910 MHz



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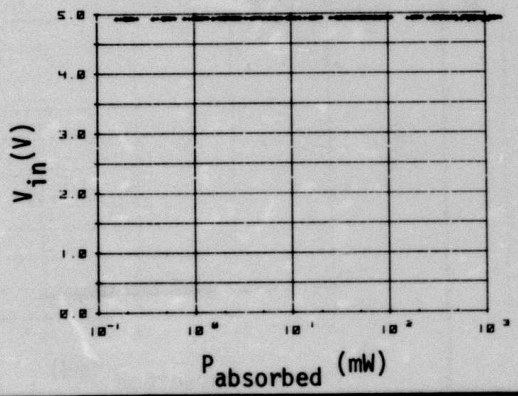
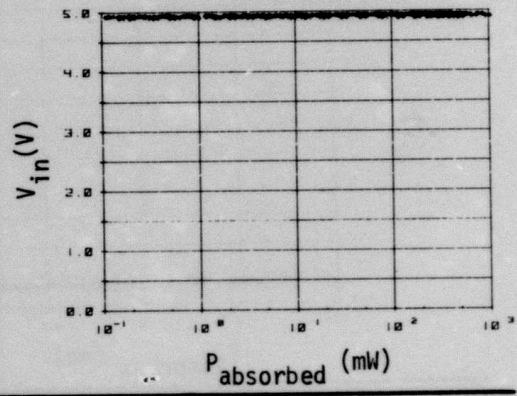
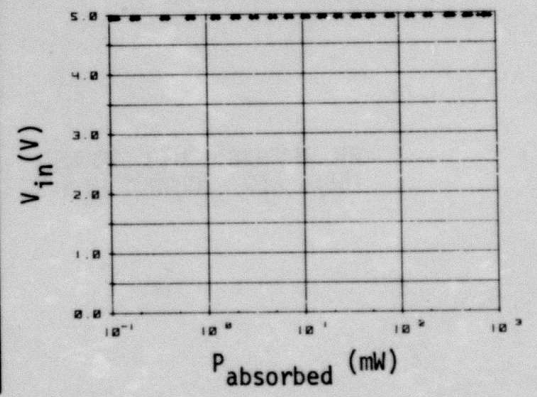


5.6 GHz



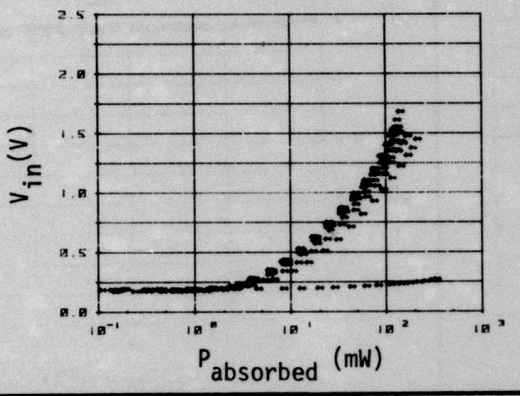
RF INJECTED INTO V_{CC}
INPUT HIGH - OUTPUT LOW

9.1 GHz

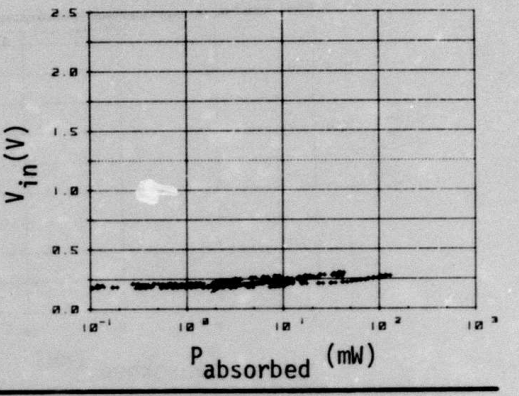


7400 INTERFERENCE DATA

220 MHz



910 MHz



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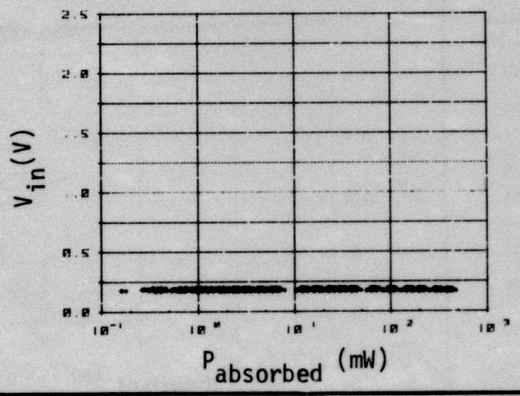
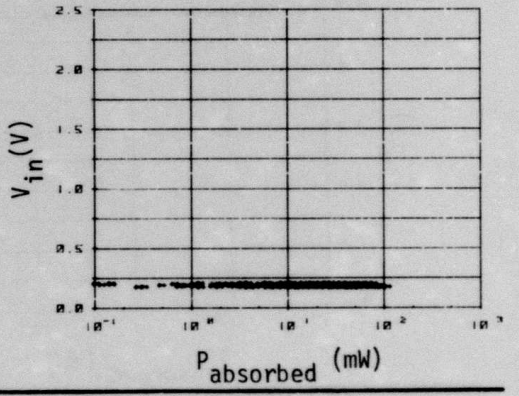
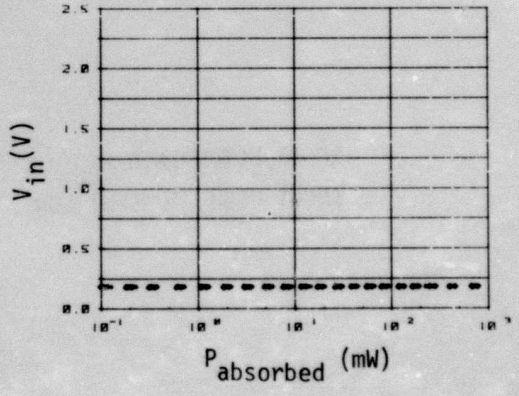


5.6 GHz



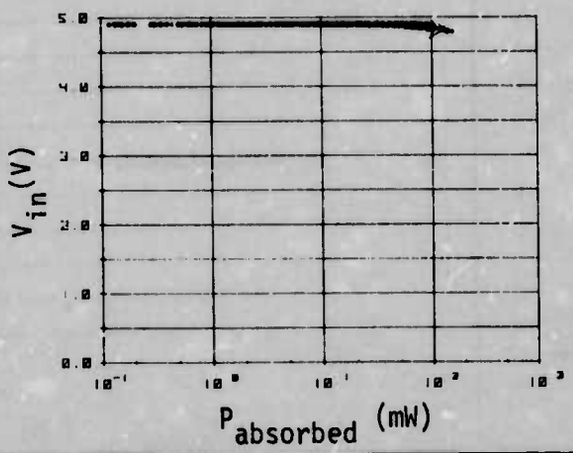
RF INJECTED INTO GROUND
INPUT LOW - OUTPUT HIGH

9.1 GHz



7400 INTERFERENCE DATA

220 MHz



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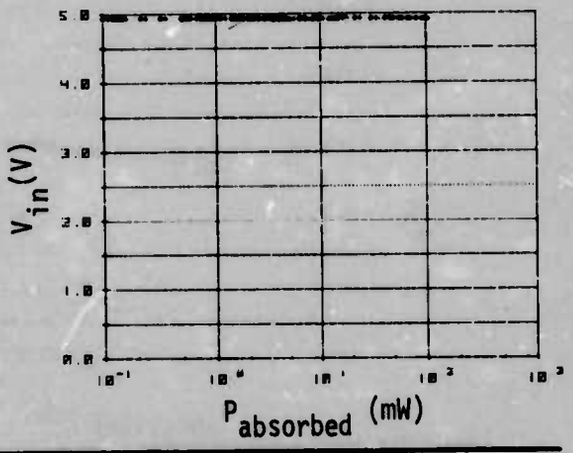

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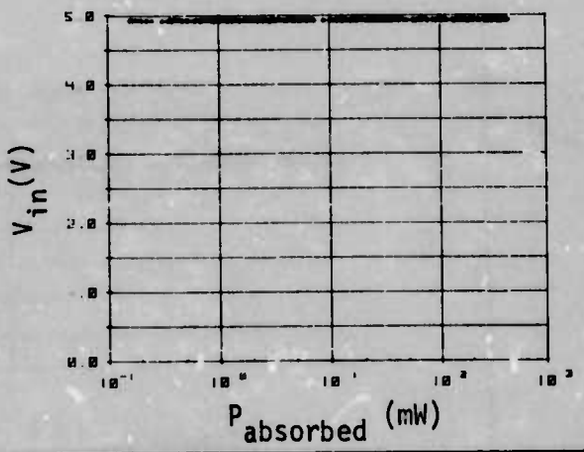

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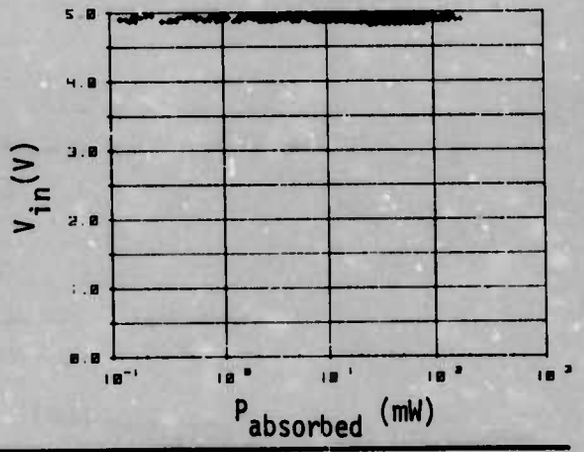
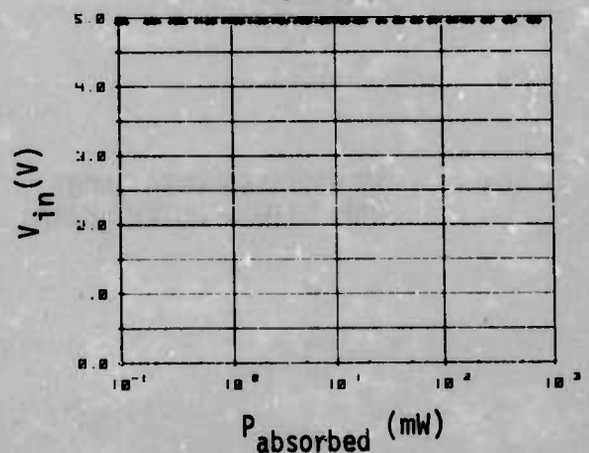


RF INJECTED INTO GROUND
INPUT HIGH - OUTPUT LOW

9.1 GHz



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ITS USE AND DISCLOSURE.

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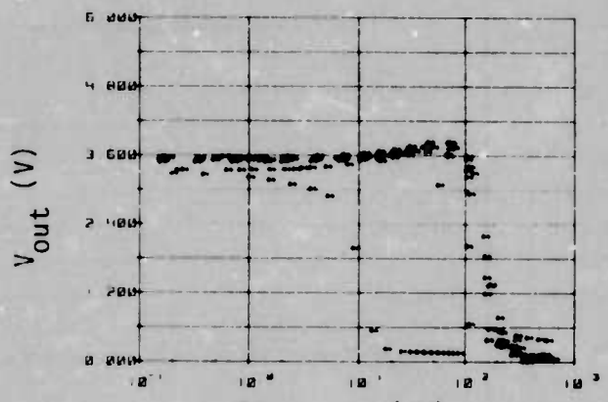
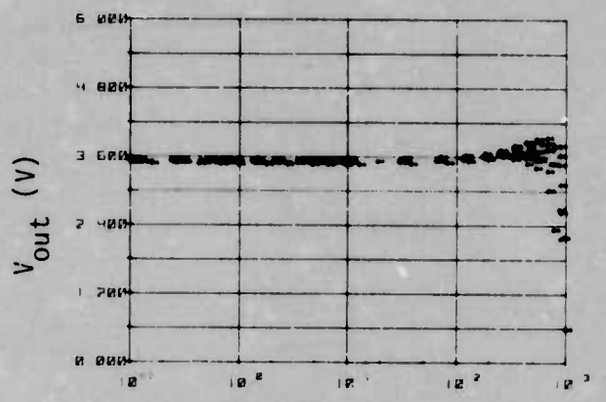
APPROVED FOR PUBLIC RELEASE;
DISTRIBUTION UNLIMITED.

7400 INTERFERENCE DATA

220 MHz



910 MHz



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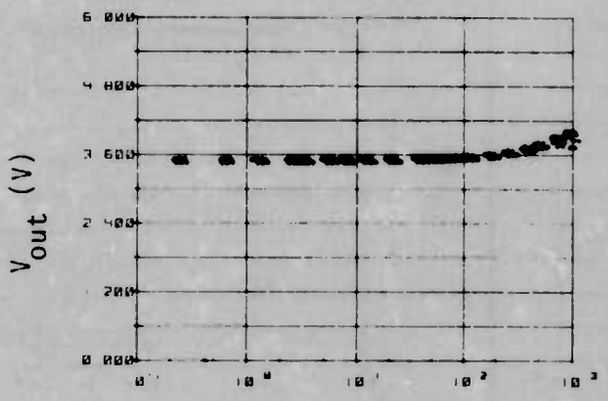
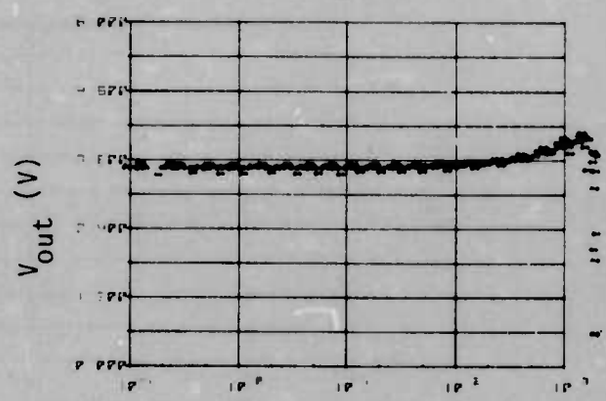
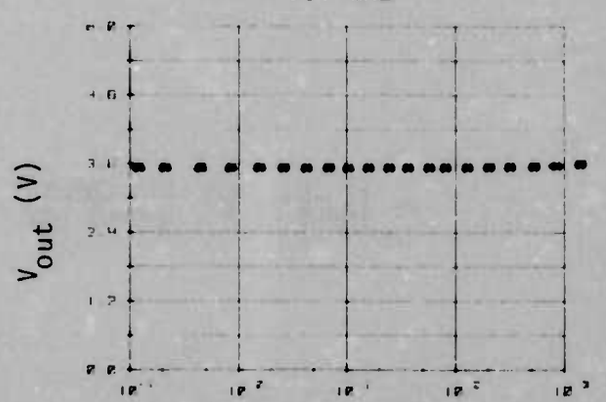


5.6 GHz



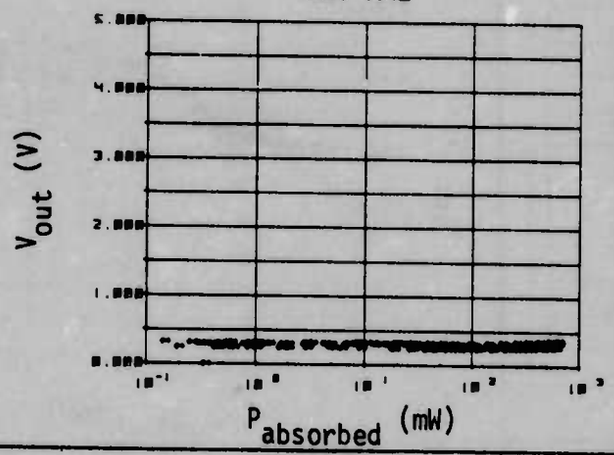
RF INJECTED INTO INPUT
INPUT LOW - OUTPUT HIGH

9.1 GHz



7400 INTERFERENCE DATA

220 MHz



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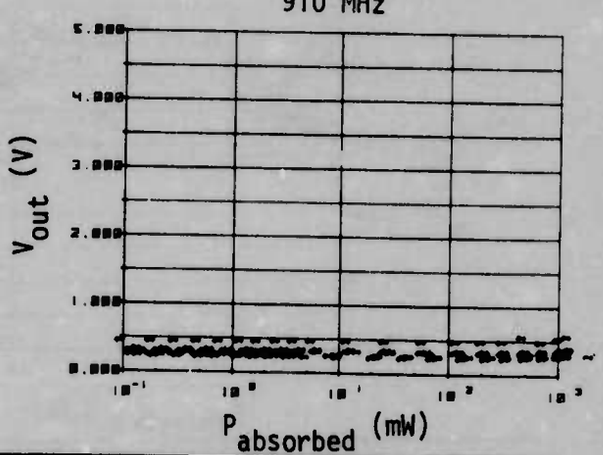
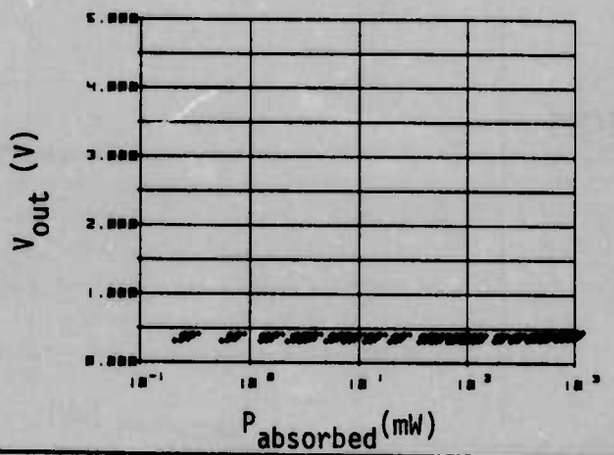
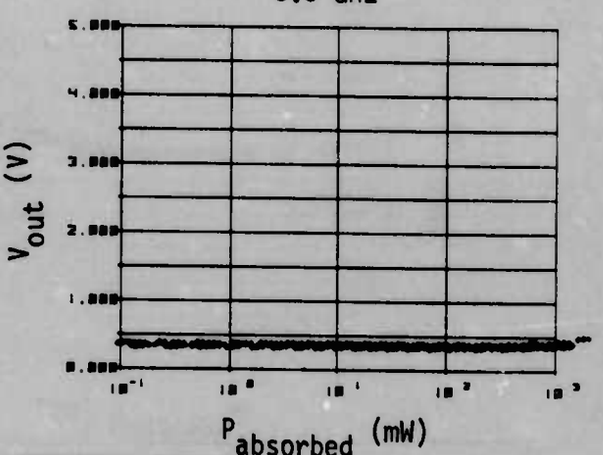


3.0 GHz

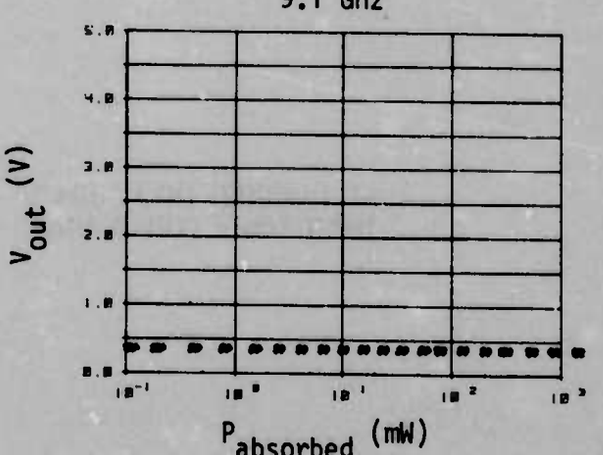


5.6 GHz



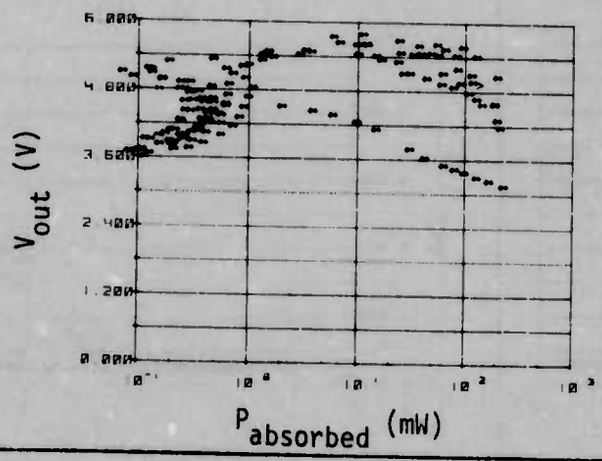
RF INJECTED INTO INPUT
INPUT HIGH - OUTPUT LOW

9.1 GHz

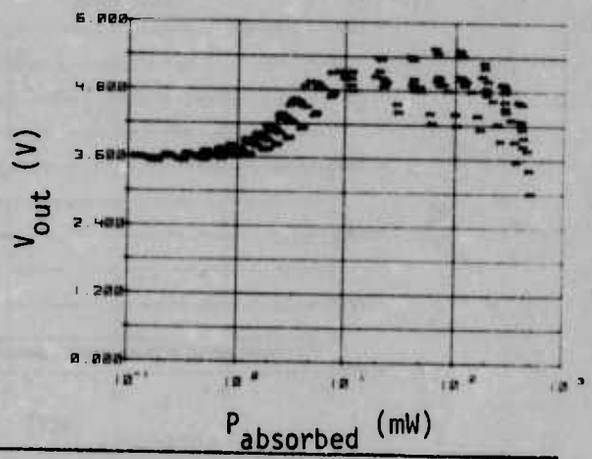


7400 INTERFERENCE DATA

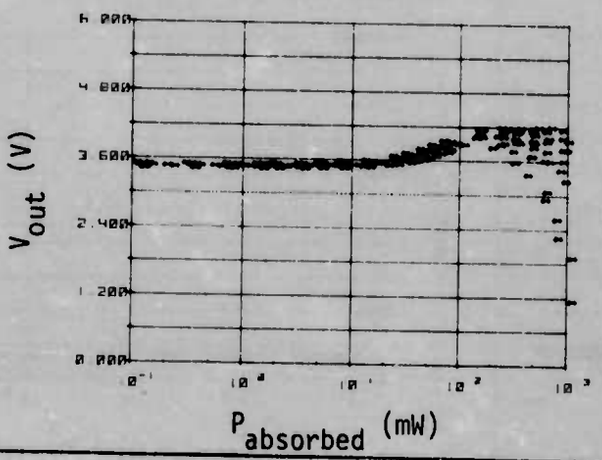
220 MHz



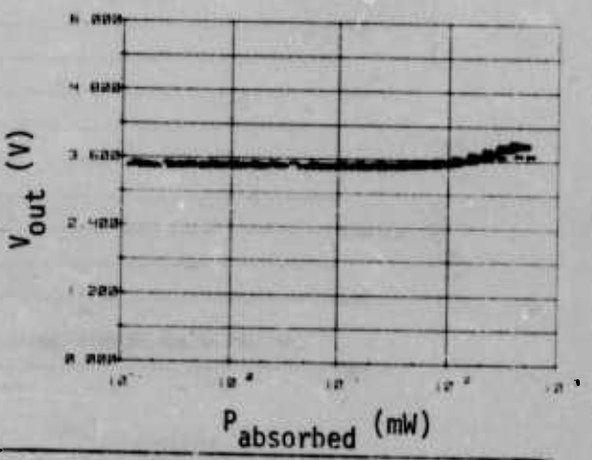
910 MHz



3.0 GHz



5.6 GHz



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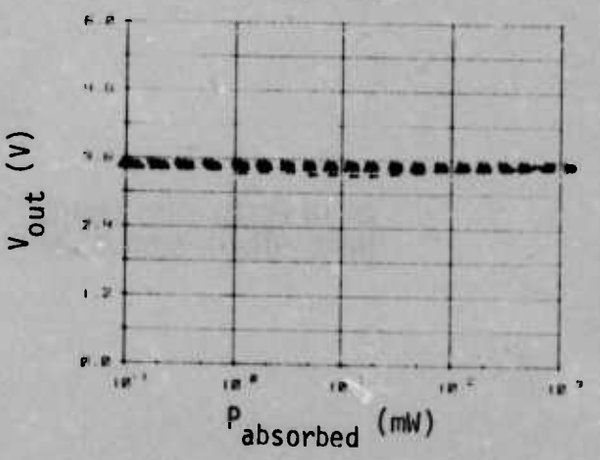
9.1 GHz



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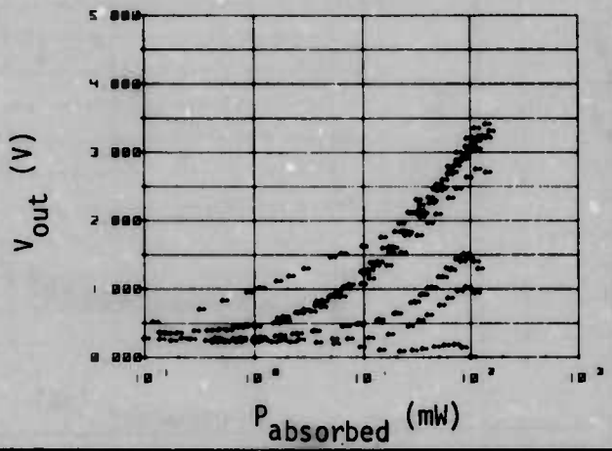

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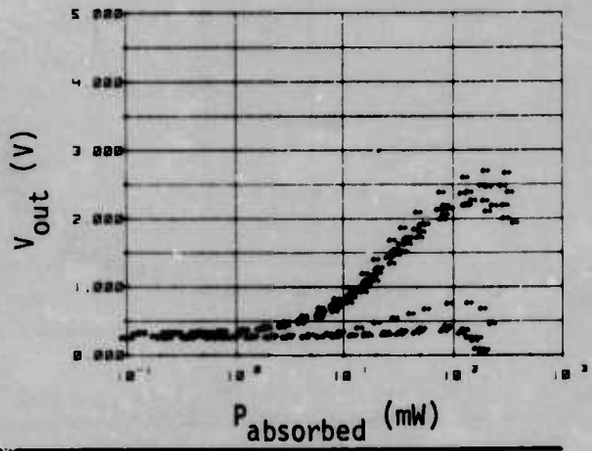

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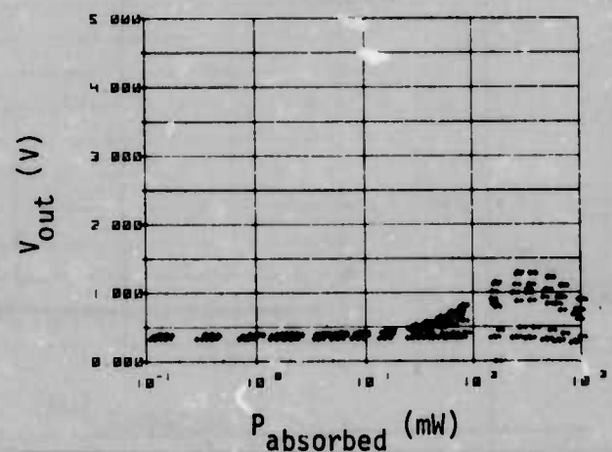

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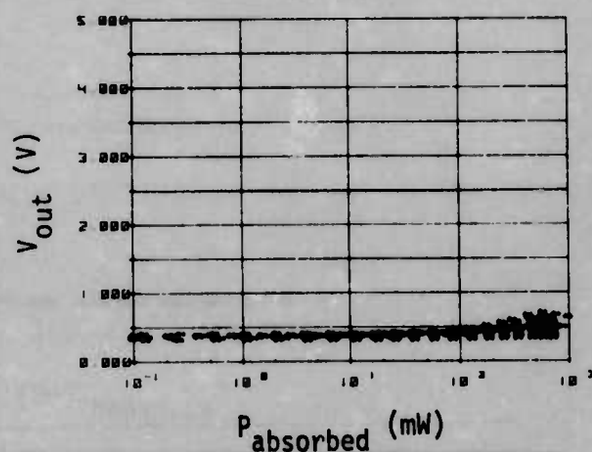
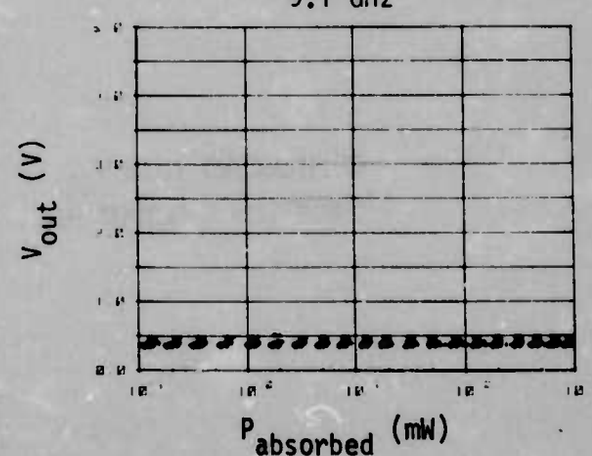


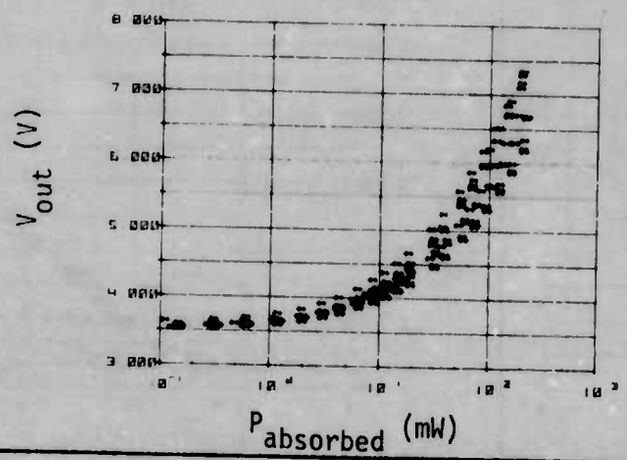
RF INJECTED INTO OUTPUT
INPUT HIGH - OUTPUT LOW

9.1 GHz



7400 INTERFERENCE DATA

220 MHz



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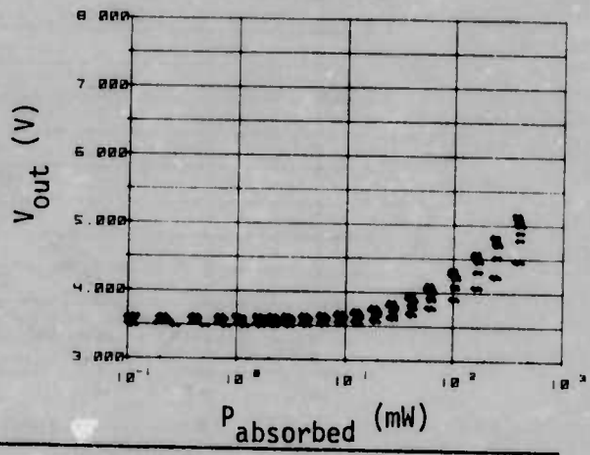

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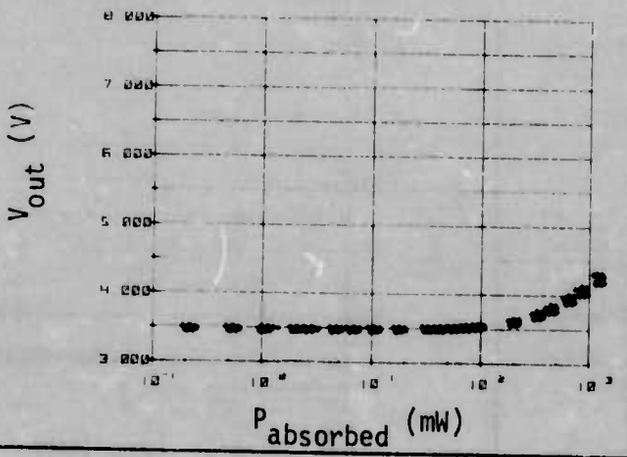
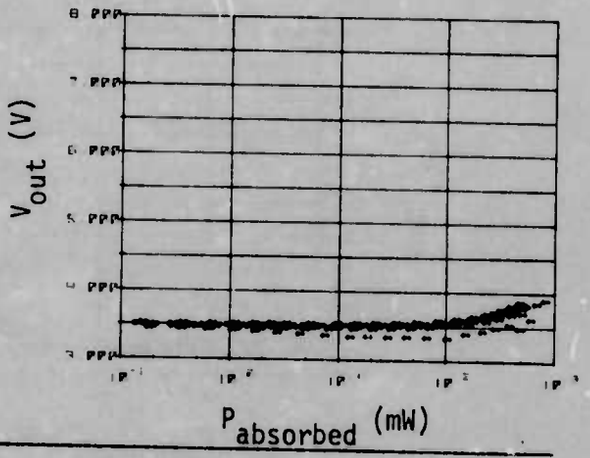
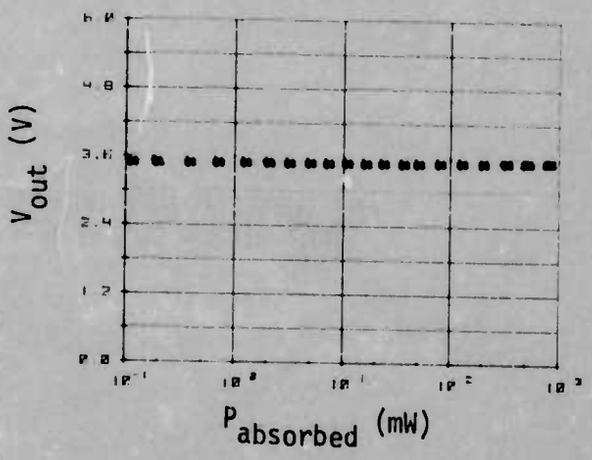


5.6 GHz



RF INJECTED INTO V_{CC}
INPUT LOW - OUTPUT HIGH

9.1 GHz



7400 INTERFERENCE DATA

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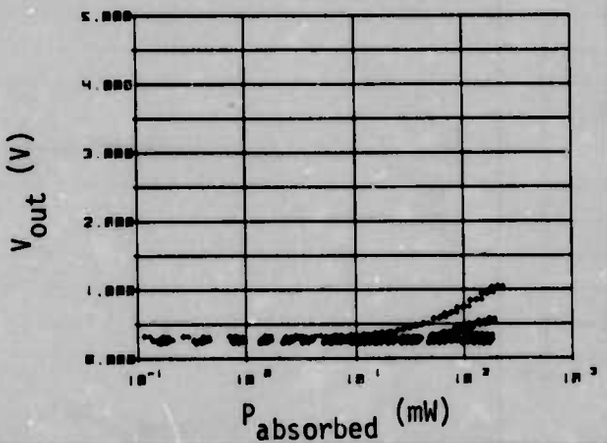
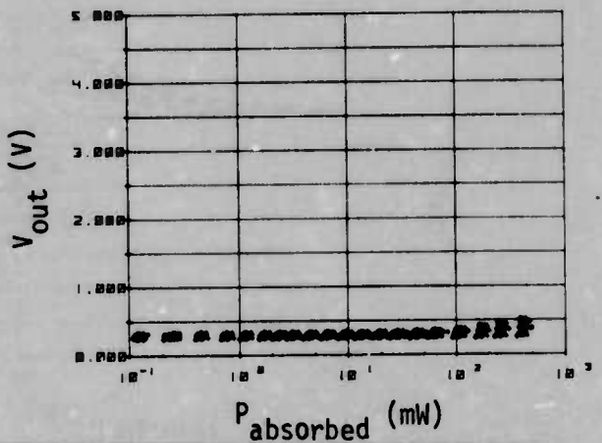


910 MHz



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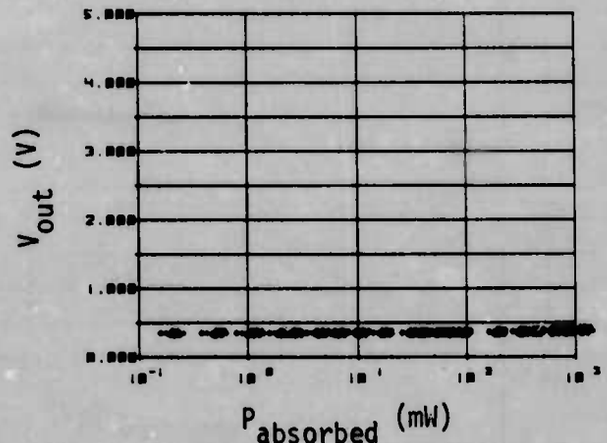

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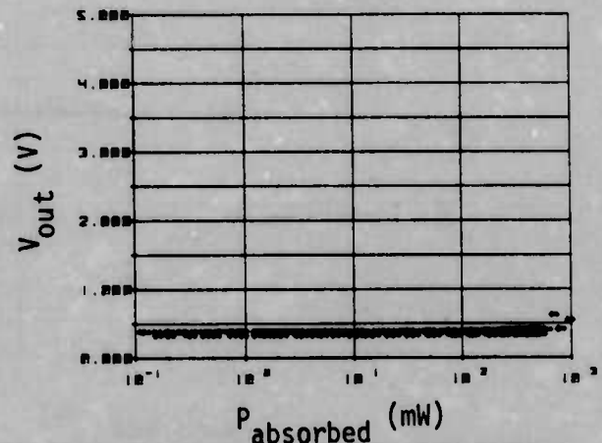
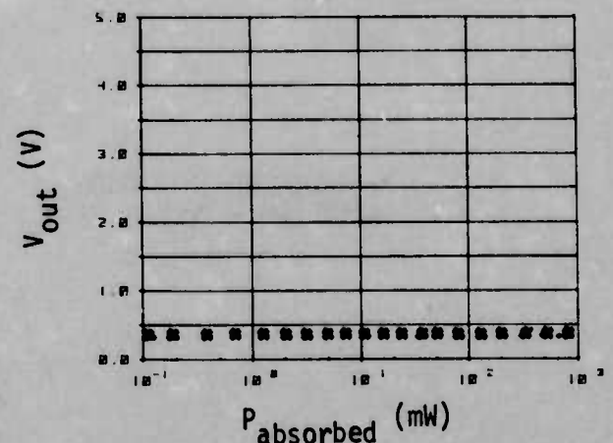


RF INJECTED INTO V_{CC}
INPUT HIGH - OUTPUT LOW

9.1 GHz



7400 INTERFERENCE DATA

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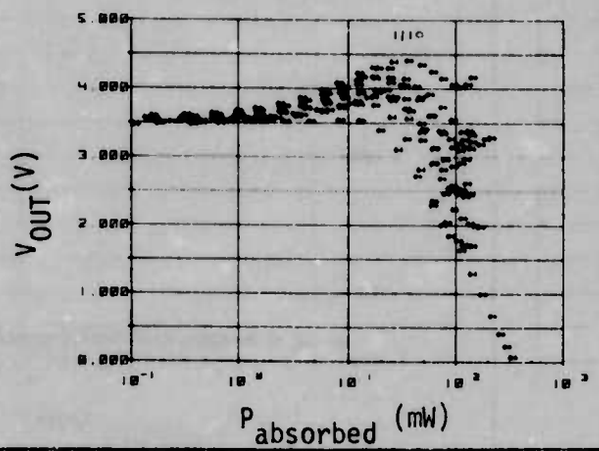
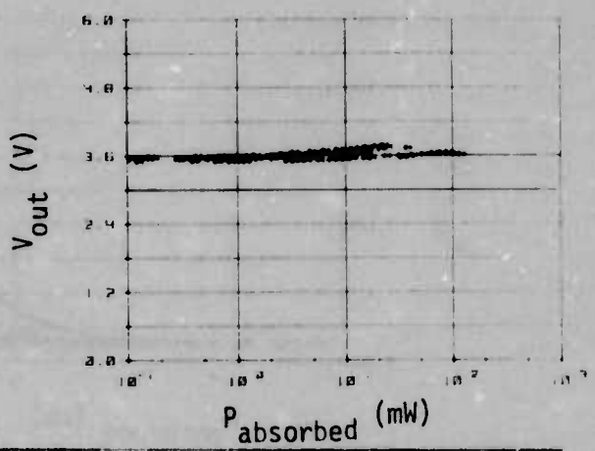


910 MHz



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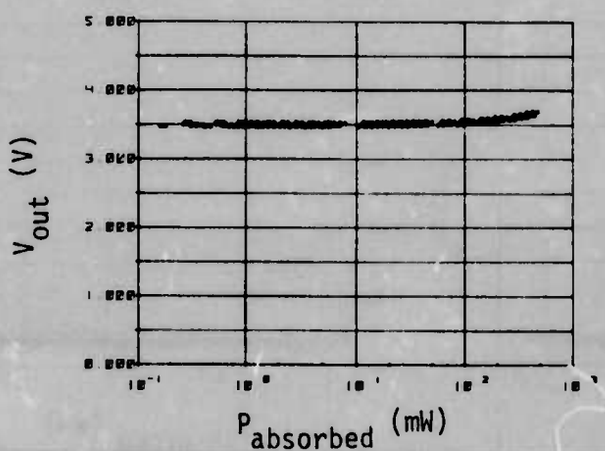

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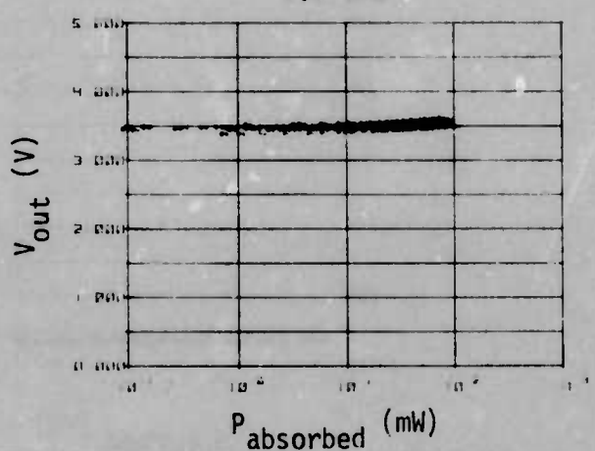
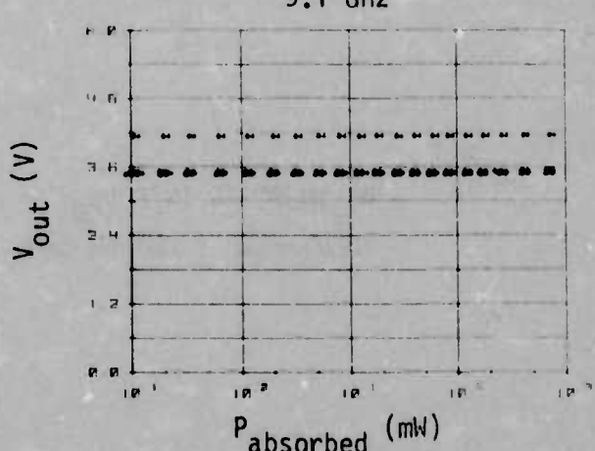


RF INJECTED INTO GND
INPUT LOW - OUTPUT HIGH

9.1 GHz



7400 INTERFERENCE DATA

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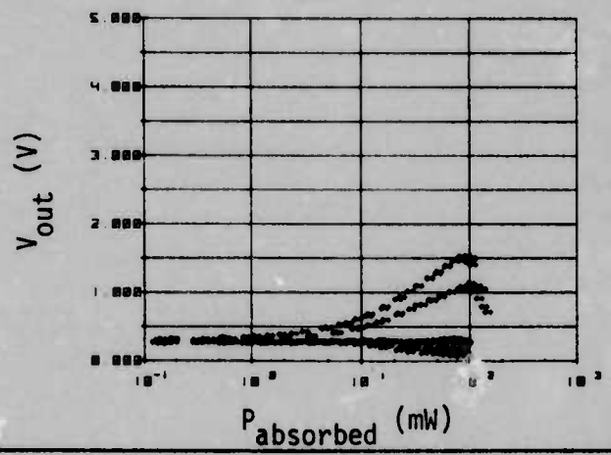

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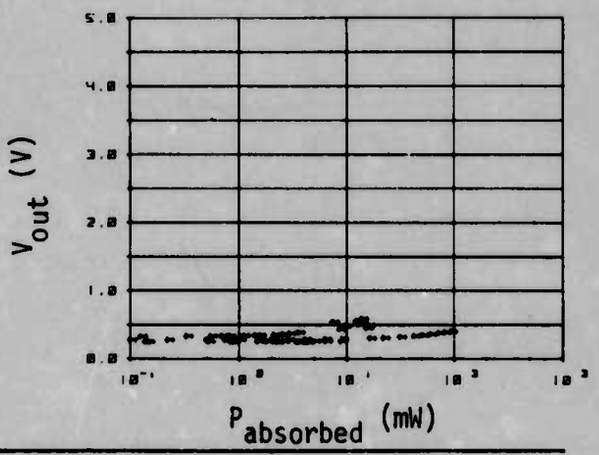

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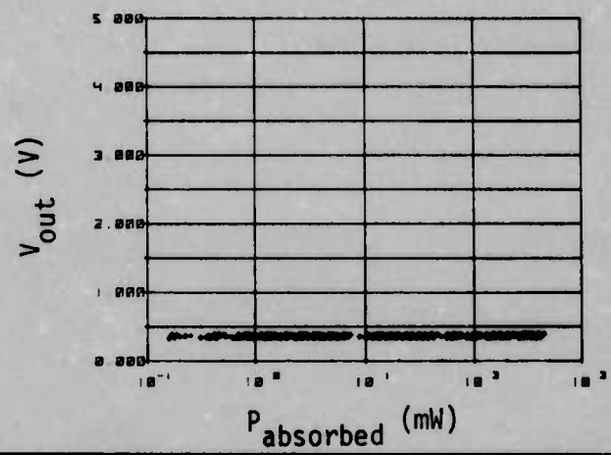

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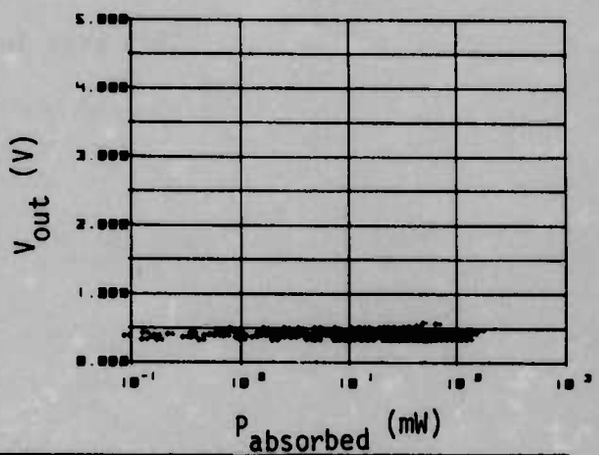
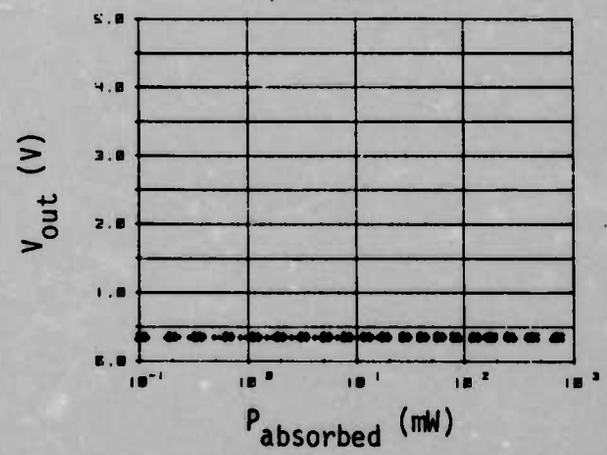


RF INJECTED INTO GND
INPUT HIGH - OUTPUT LOW

9.1 GHz



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